

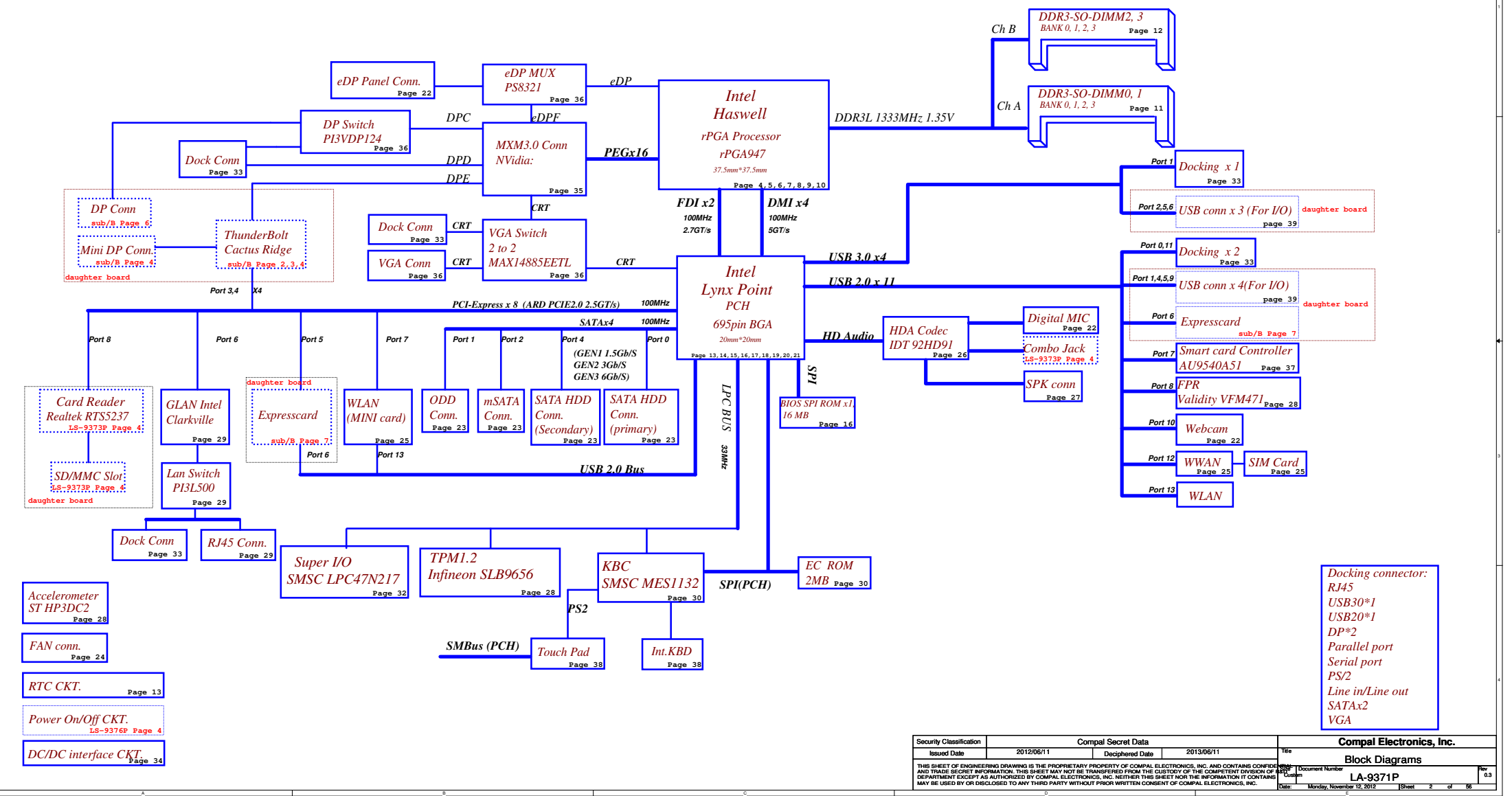
# Compal Confidential

## Intel Haswell rPGA Processor with Lynx Point-H Afterburn MXM LA-9371P

2012-11-12

REV : 0.3

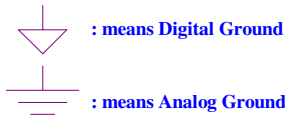
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	
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Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

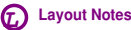
Symbol Note :



@ : means just reserve , no build

AMT@ : means just install for support iAMT

CONN@ : means ME part.



Layout Notes

07/24 update



: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable.Remove before MP

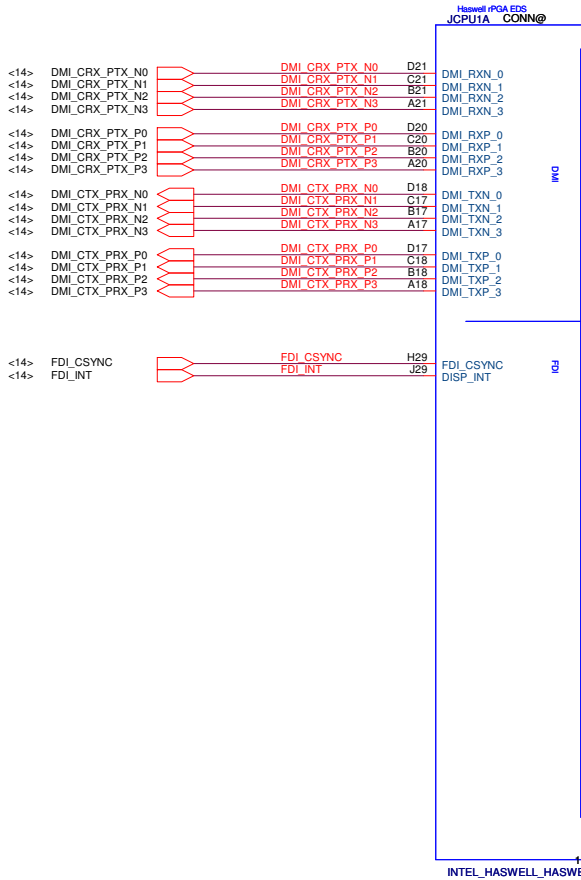
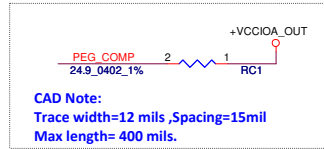
SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

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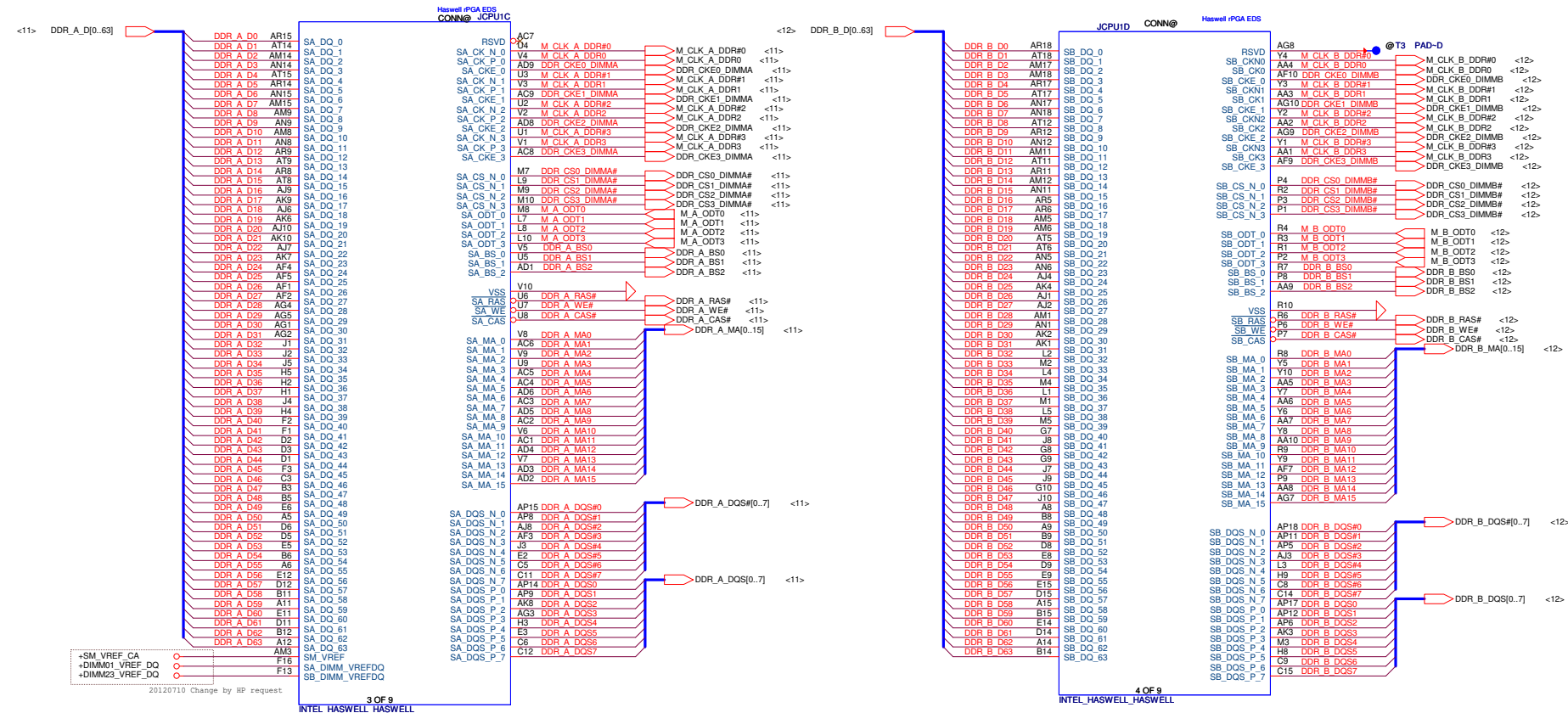


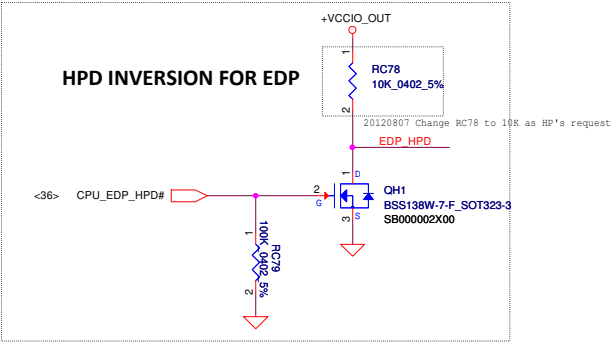
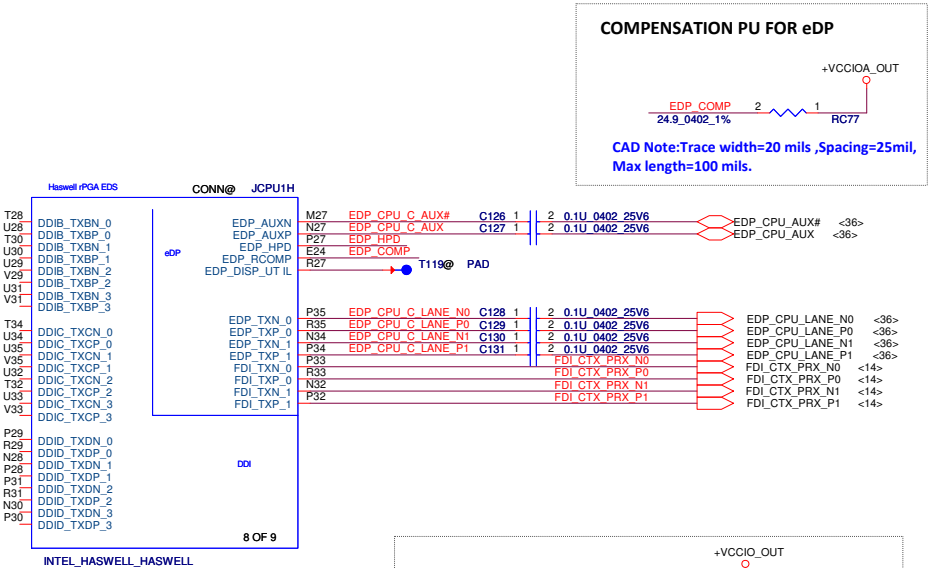
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PEG_RXN_3	L30	PEG_CRX_GTX_N3
PEG_RXN_4	M33	PEG_CRX_GTX_N4
PEG_RXN_5	L32	PEG_CRX_GTX_N5
PEG_RXN_6	M35	PEG_CRX_GTX_N6
PEG_RXN_7	L34	PEG_CRX_GTX_N7
PEG_RXN_8	E29	PEG_CRX_GTX_N8
PEG_RXN_9	D28	PEG_CRX_GTX_N9
PEG_RXN_10	E31	PEG_CRX_GTX_N10
PEG_RXN_11	D30	PEG_CRX_GTX_N11
PEG_RXN_12	E35	PEG_CRX_GTX_N12
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PEG_RXP_3	K30	PEG_CRX_GTX_P3
PEG_RXP_4	L33	PEG_CRX_GTX_P4
PEG_RXP_5	K32	PEG_CRX_GTX_P5
PEG_RXP_6	L35	PEG_CRX_GTX_P6
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PEG_TXP_4	H31	PEG_CTX_GRX_C_P4
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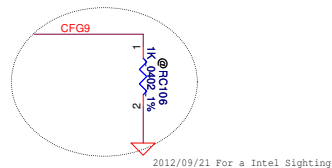
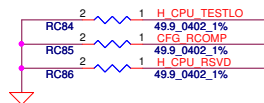
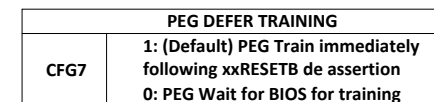
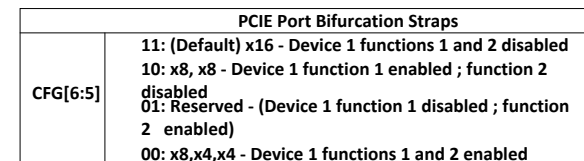
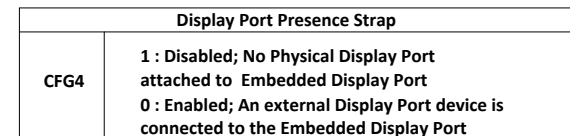
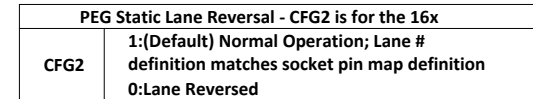
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PEG_CTX_GRX_C_N15	CC32 1	2 0.22U 0402 6.3V6K PEG_CTX_GRX_N15



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Issued Date	2012/06/11	Deciphered Date	2013/06/11	PM,XDP,CLK
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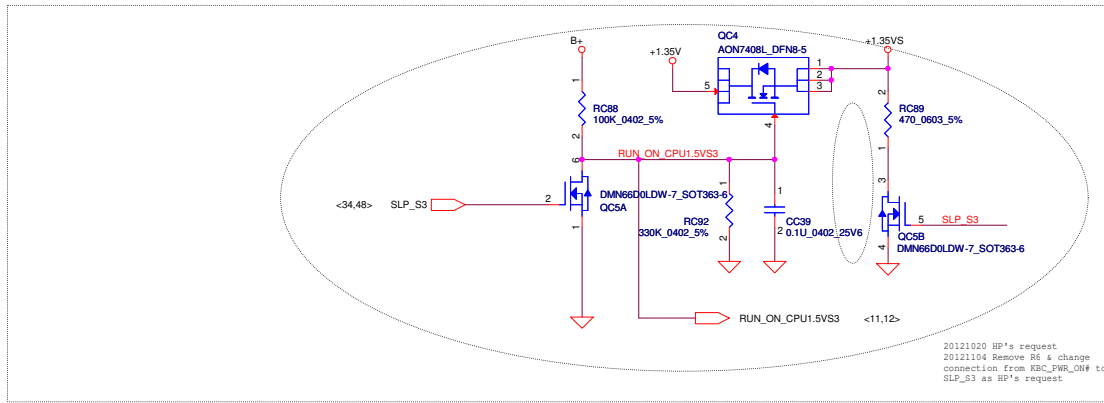








+1.35VS Source



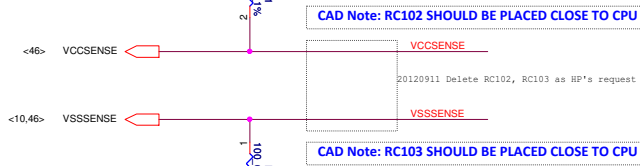
## SVID ALERT

CAD Note: Place the PU resistors close to CPU  
RC60 close to CPU 300 - 1500mils

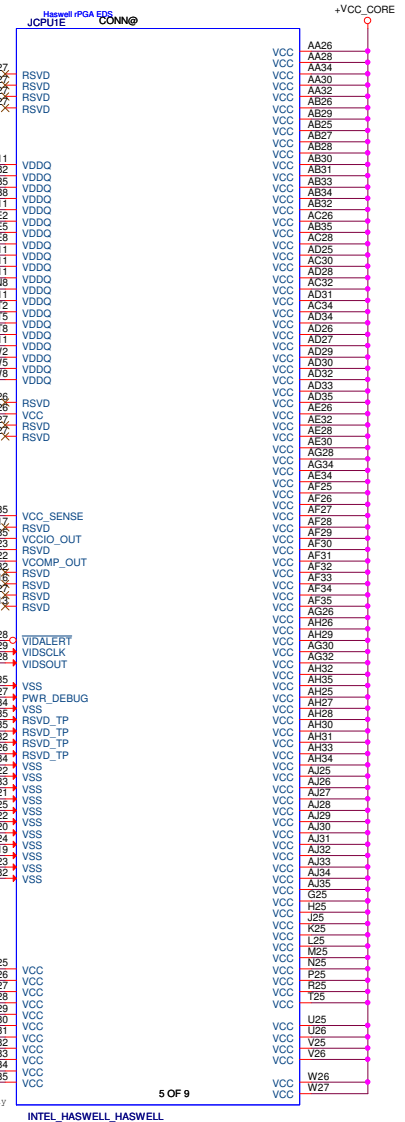
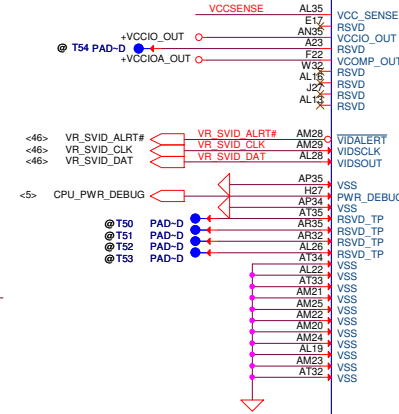
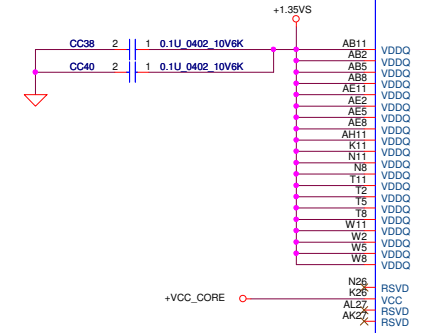
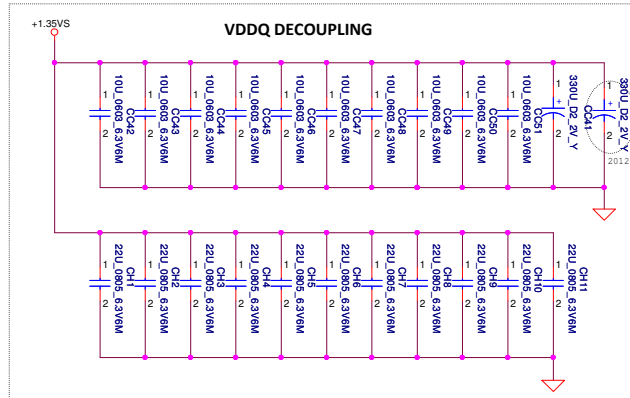
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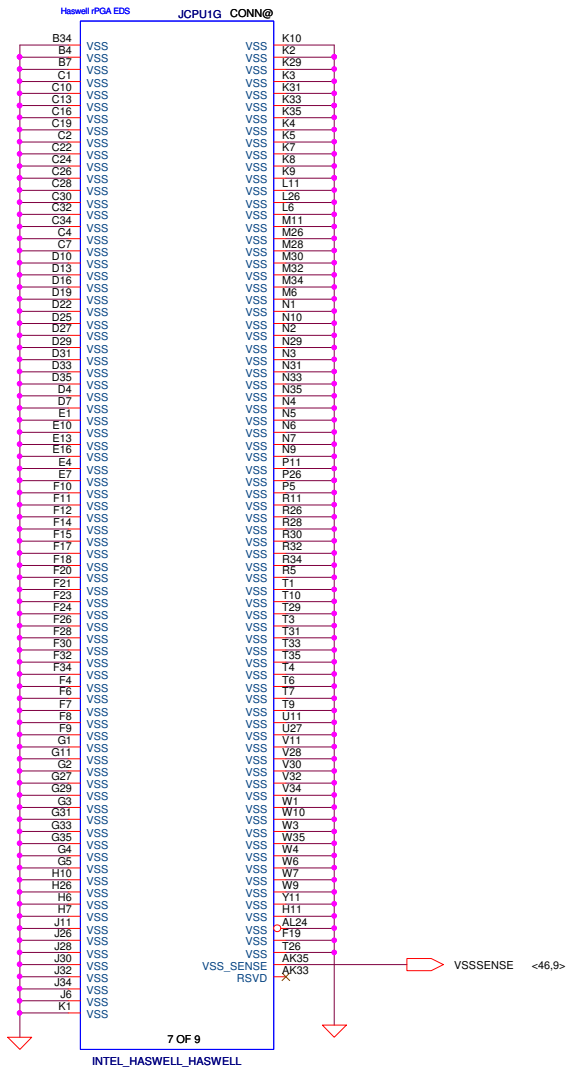
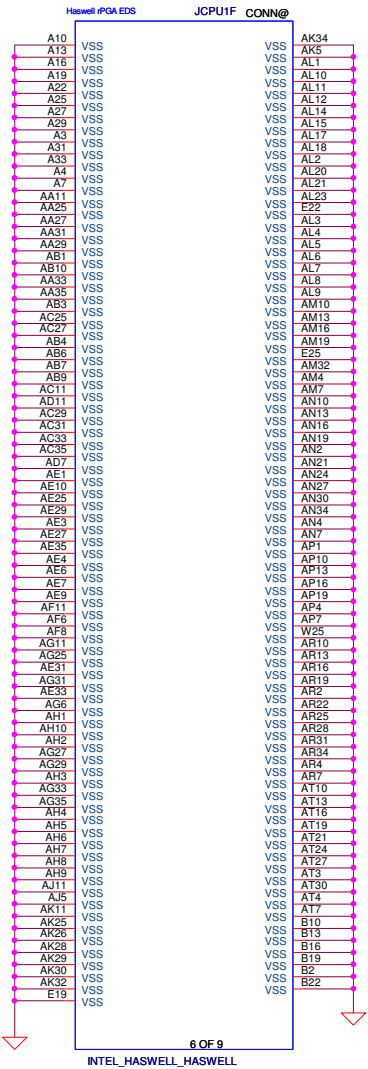
CAD Note: Place the PU resistors close to CPU  
RC63 close to CPU 300 - 1500mils

## VCC\_SENSE



## VDDQ DECOUPLING

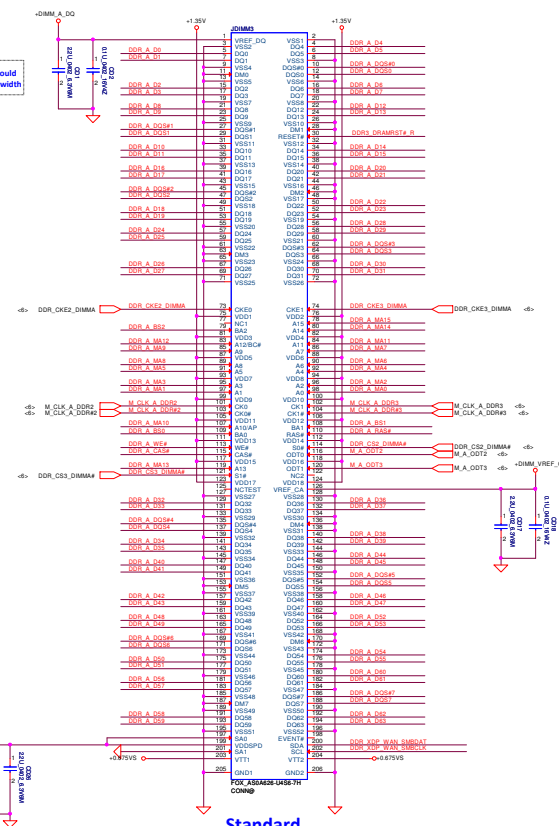




## JDIMM3 H=4.0mm BOT



All VREF traces should have 10 mil trace width



## Standard

Reverse

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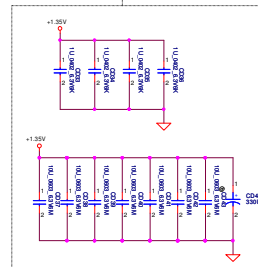
Populate R04, De-Populate R08 for Intel DDR3 VREFDQ multiple methods M1  
Populate R06, De-Populate R04 for Intel DDR3 VREFDQ multiple methods M3

# JDIMM2 H=9.2mm TOP

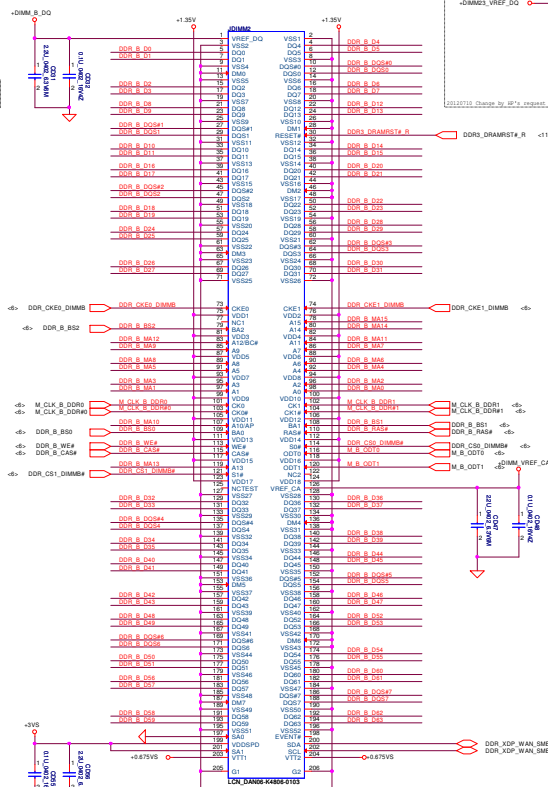
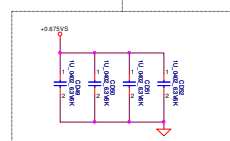
# JDIMM4 H=4.0mm BOT

DDR\_B\_DQ[43]  
DDR\_B\_DQS[9..7]  
DDR\_B\_DQS[9..7]  
DDR\_B\_M[15]

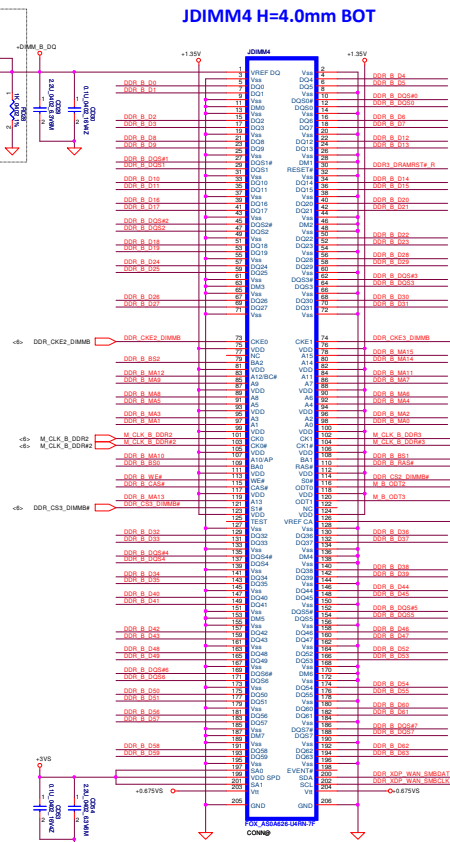
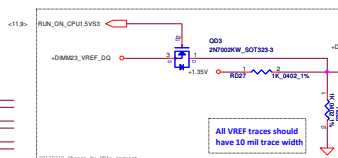
Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIMM2,203,204

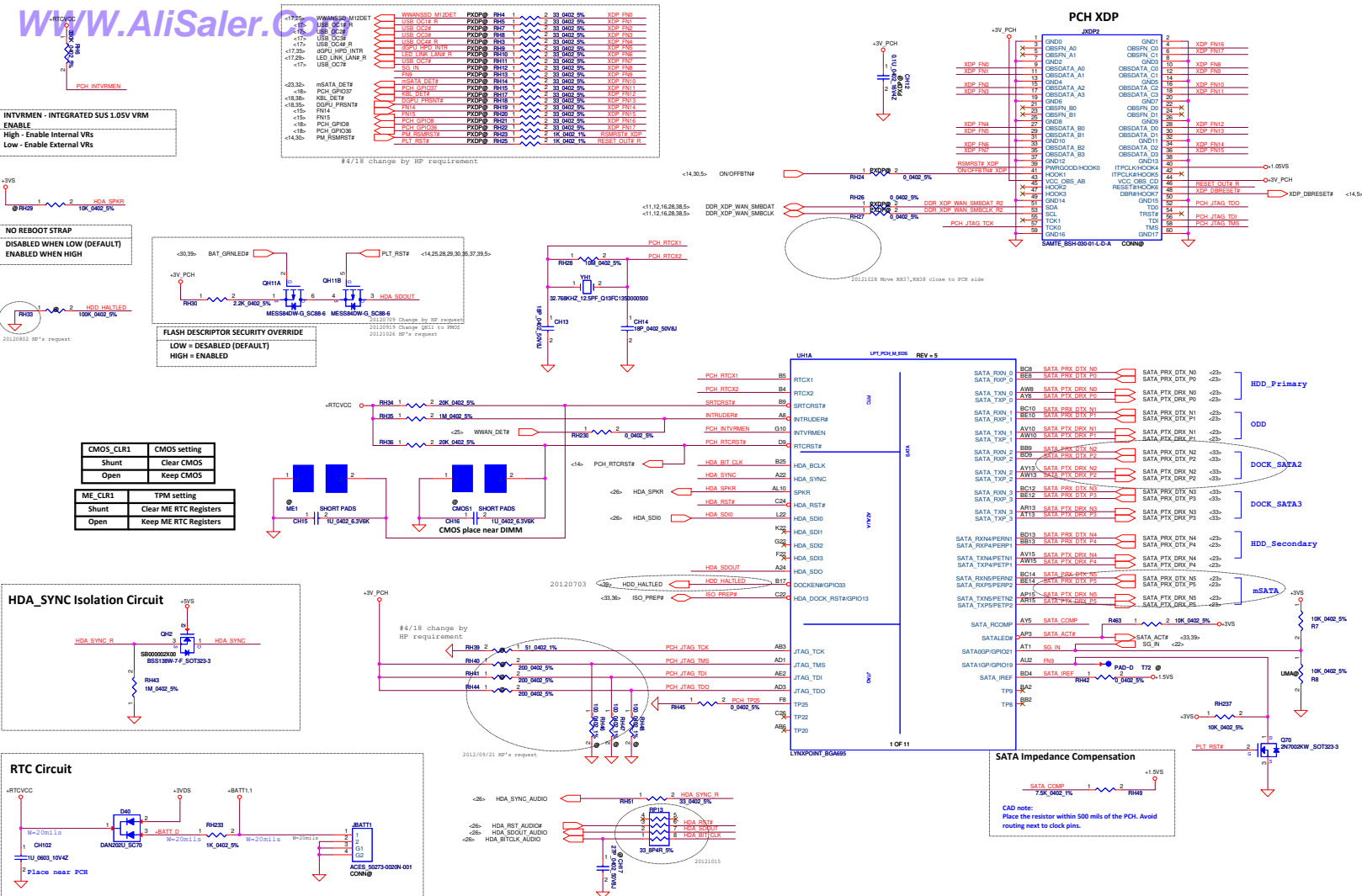


Reverse



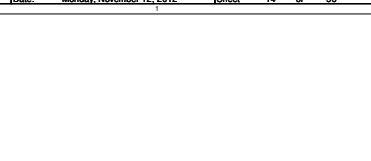
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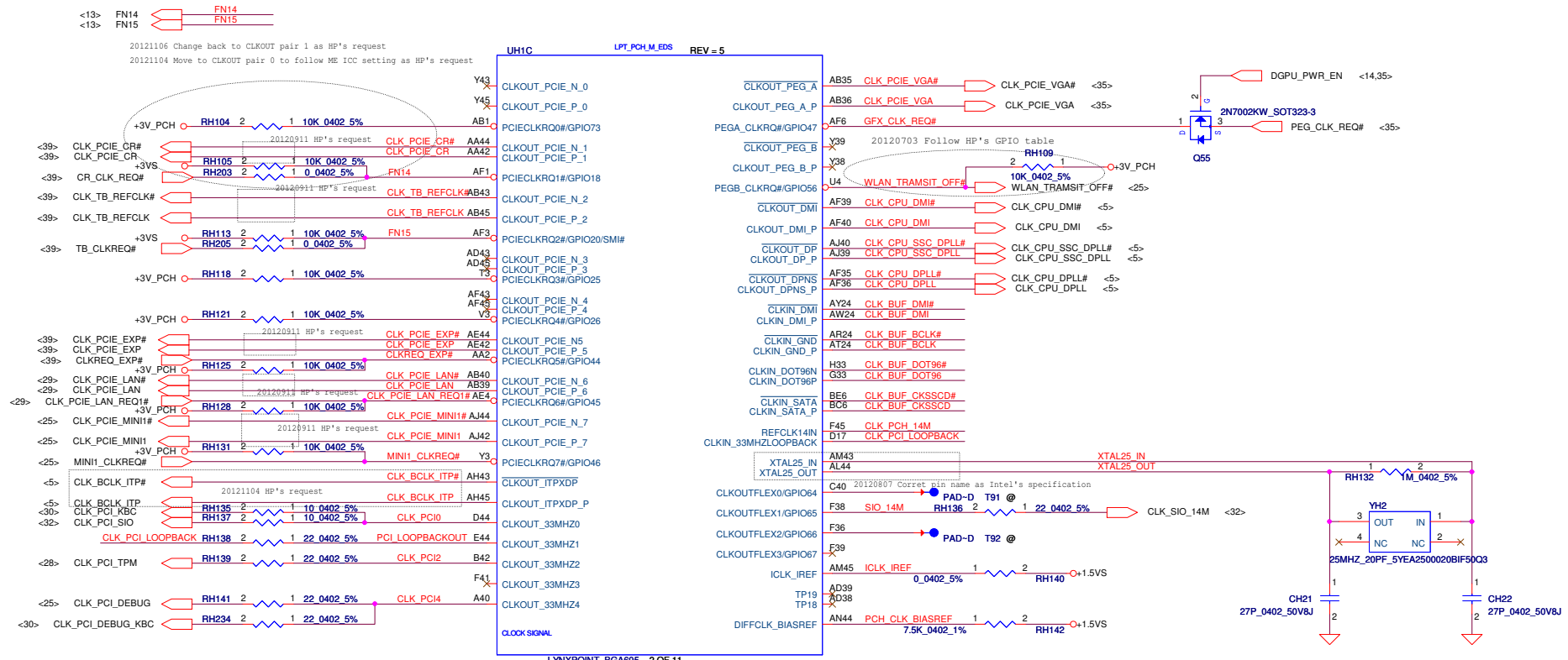
Security Classification		Compul Secret Data		Compul Electronics, Inc.	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	DDRIII DIMM3&4	
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Rev.		Mod.		Ver.	1.0



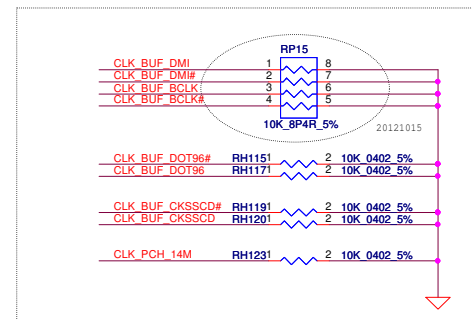


3		
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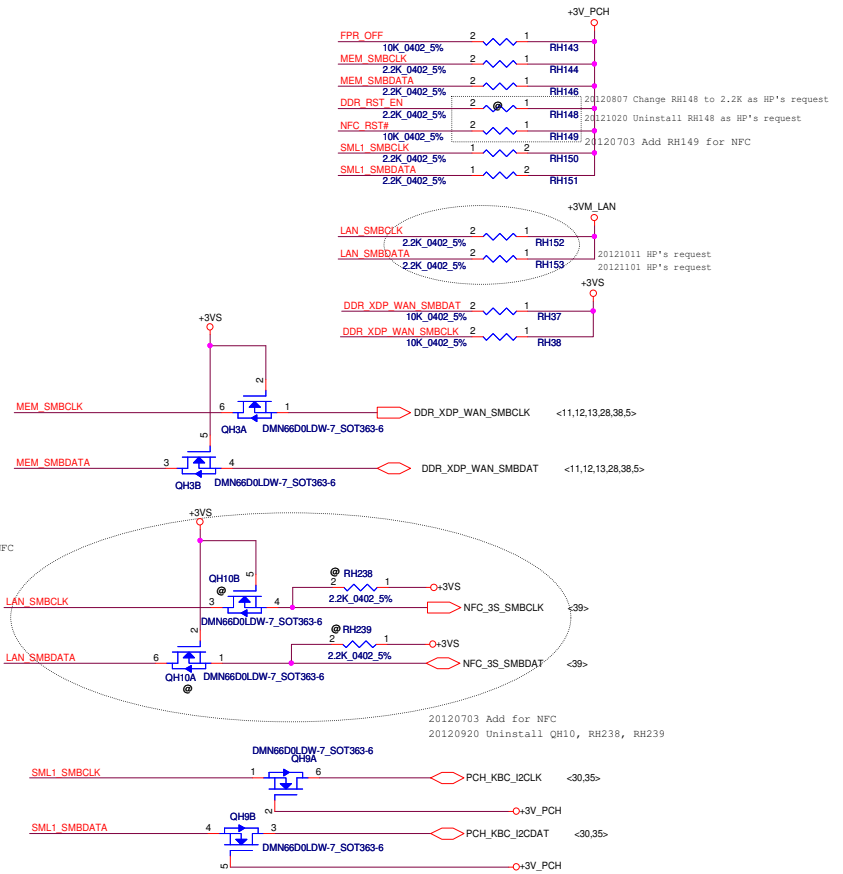
PCIECLK REQ Pull UP Power Rail:  
SUS Rail : 0 3 4 5 6 7  
Core Rail: 1 2



CLOCK TERMINATION for FCIM and need close to PCH

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Deciphered Date				2013/06/11				PCH- CLK			
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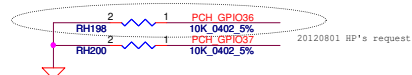
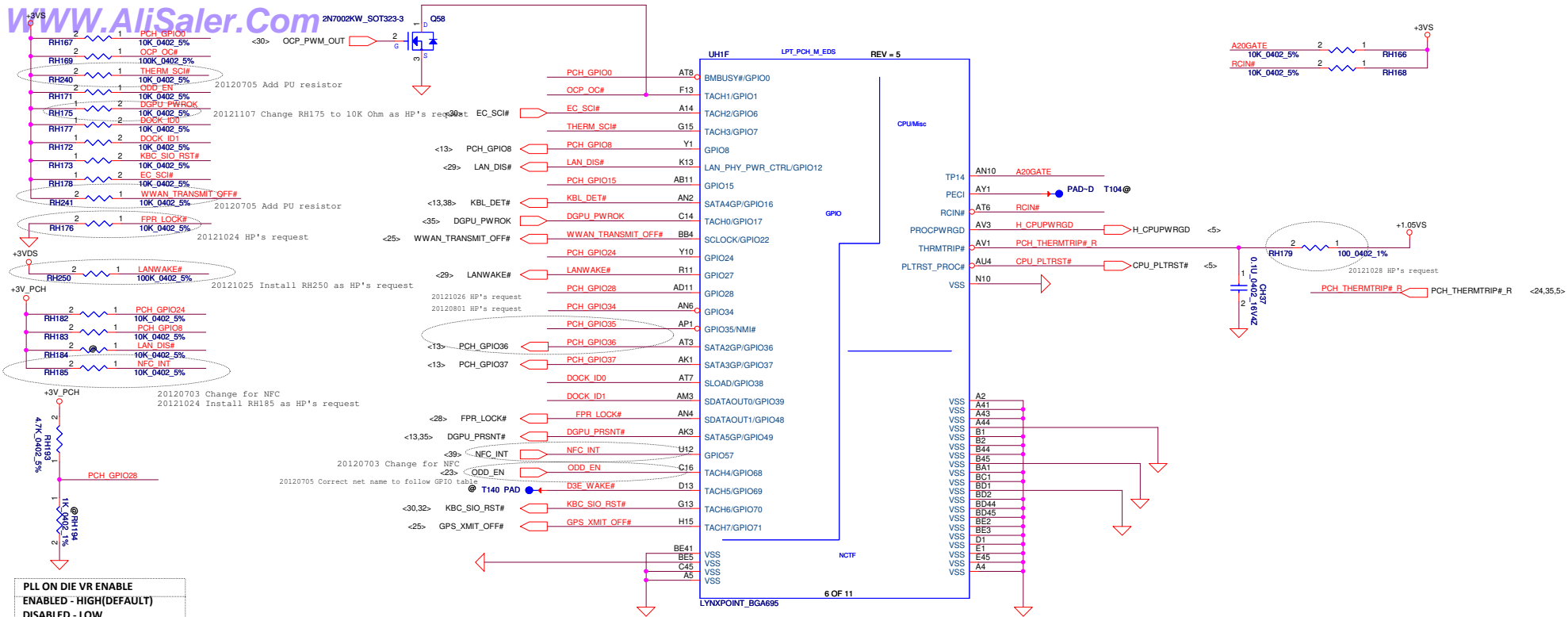




5	4	3	2	1
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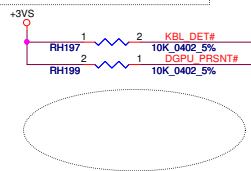




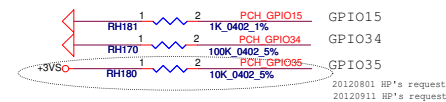


SATA2GP/GPIO36, SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.  
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER  
PLRST\_N DE-ASSERTS).  
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01



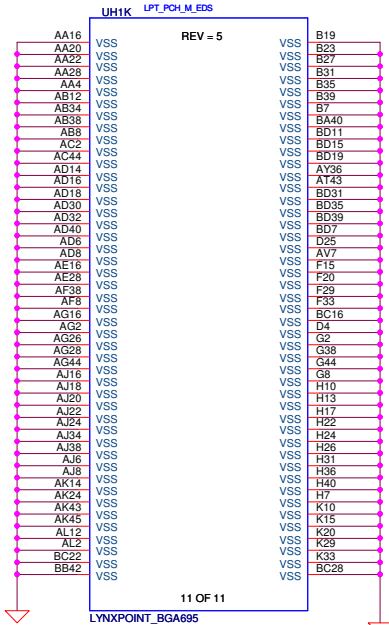
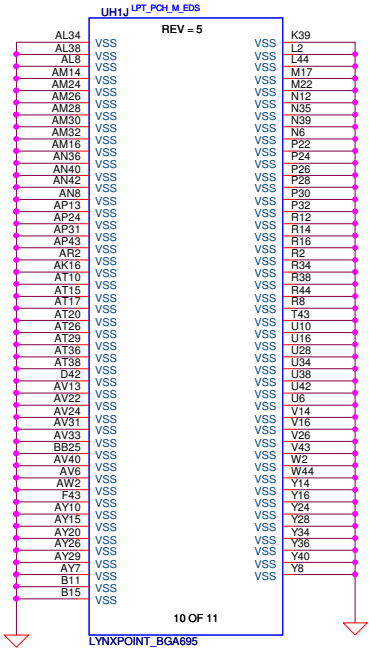
Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3
				(00)	(00)							(00)	(00)				
				USB3_3	USB3_4							PCIE_1	PCIE_2				



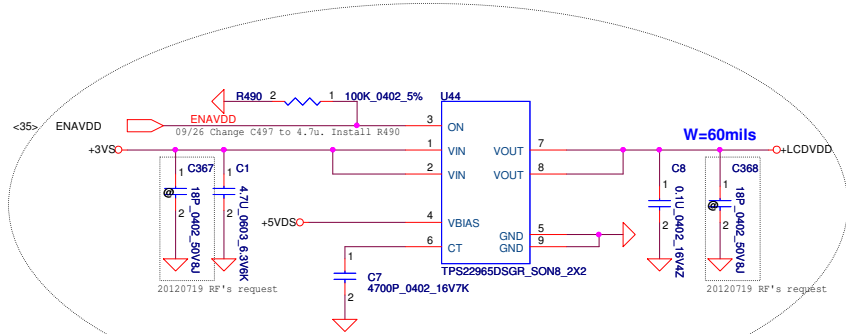
Board ID	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
PV1	1	0	0	0
MV	1	1	0	0



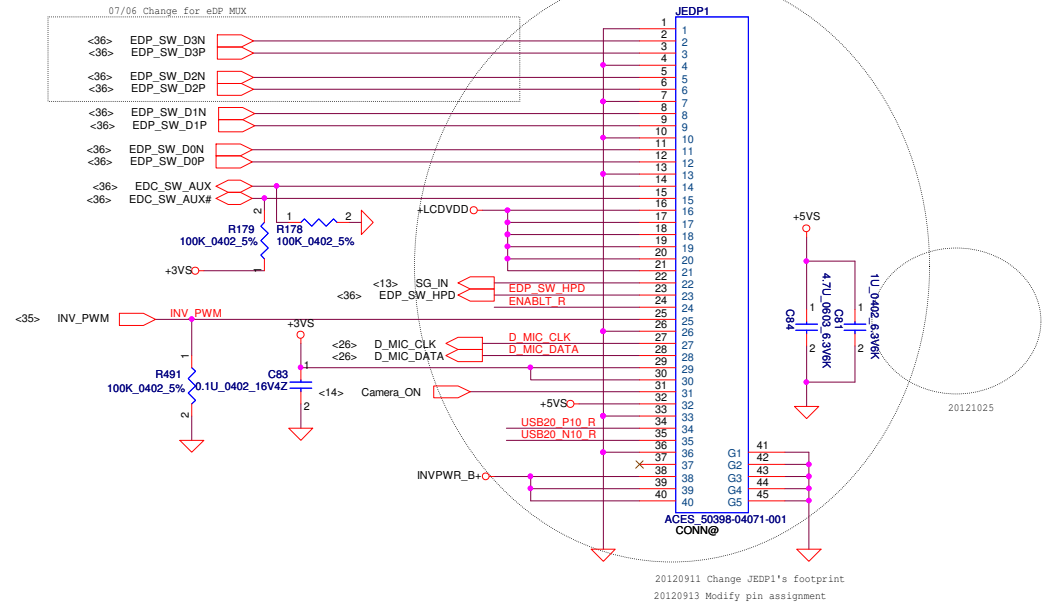
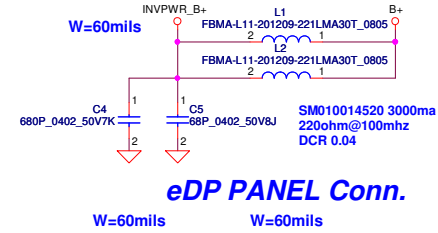
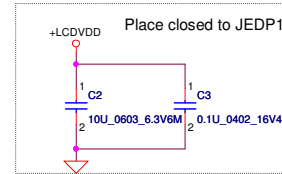
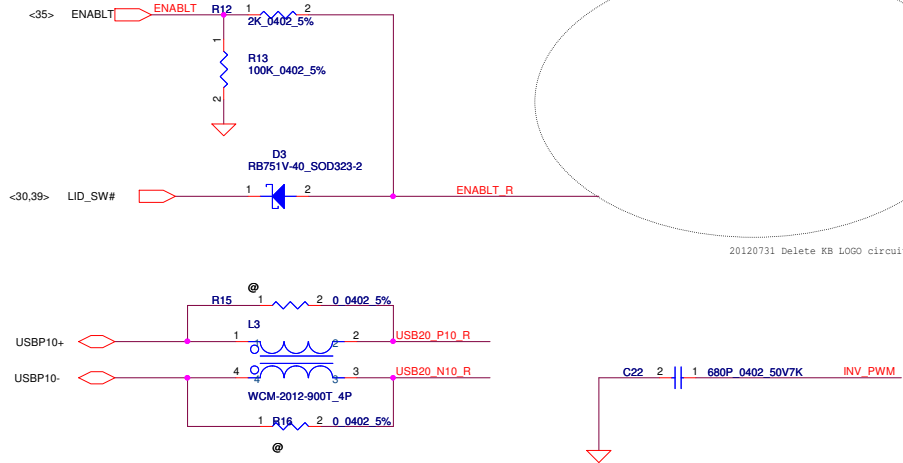




# LCD POWER CIRCUIT

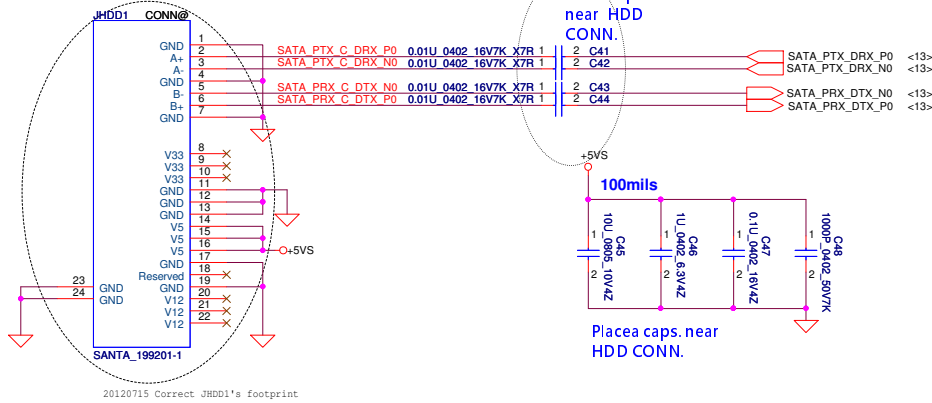


20121026 Change LCDVDD power rail solution.  
Delete R9,R10,R11,C6,Q12,Q20

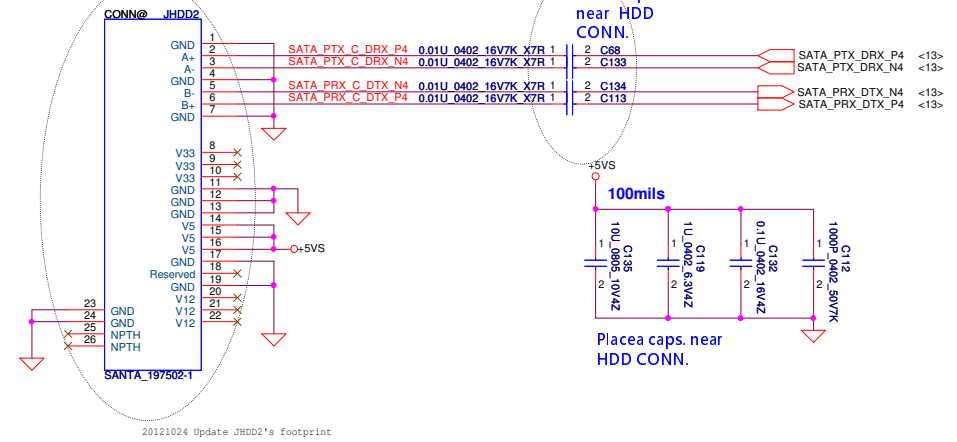


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				Date:	Monday, November 12, 2012
				Sheet	22 of 56
				Rev	0.3

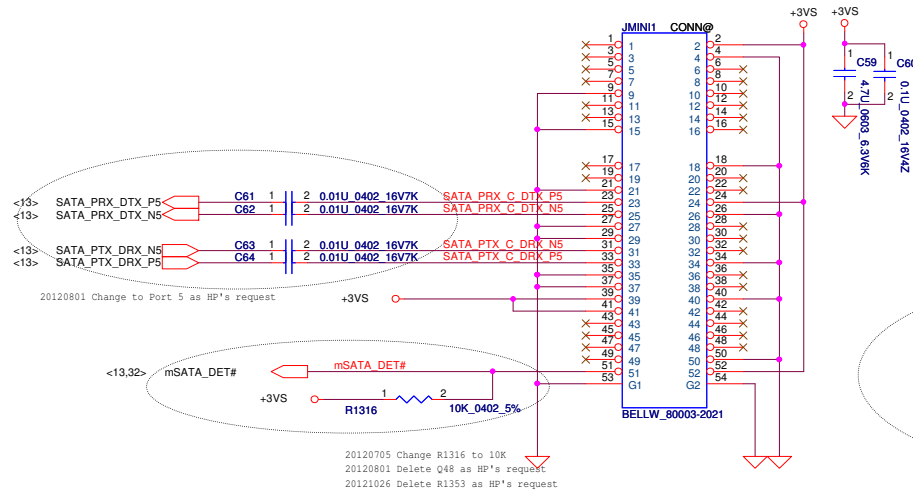
### SATA Primary HDD CONN.



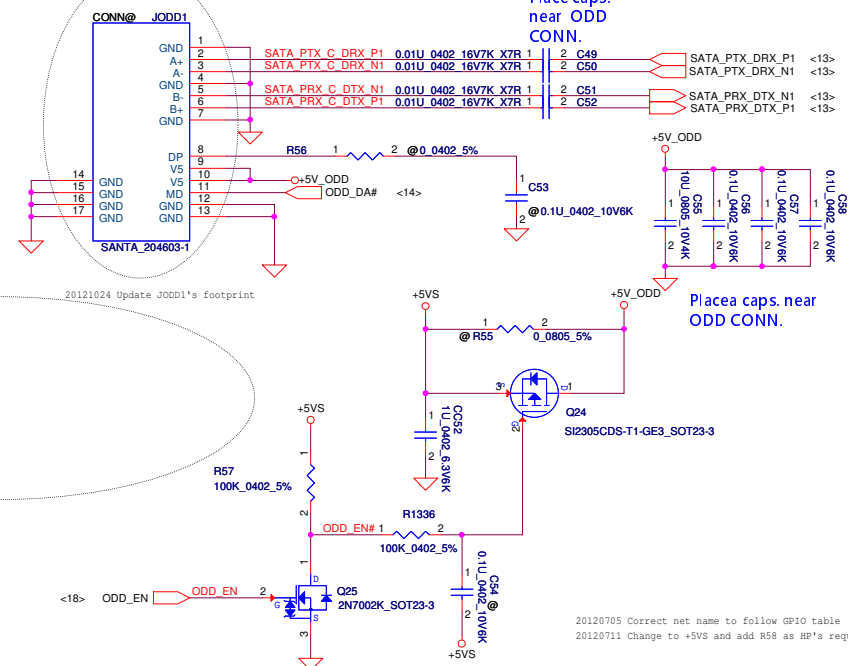
### SATA Second HDD CONN.



### mSATA Conn.

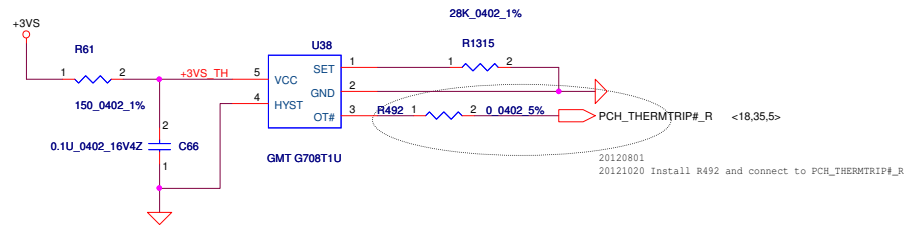
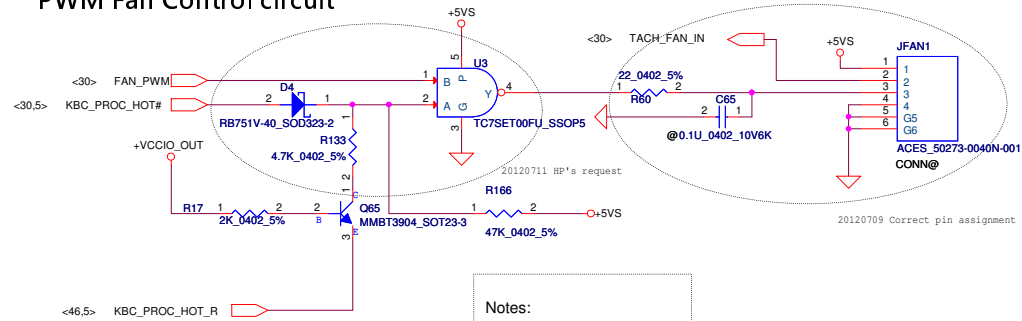


### SATA ODD CONN.



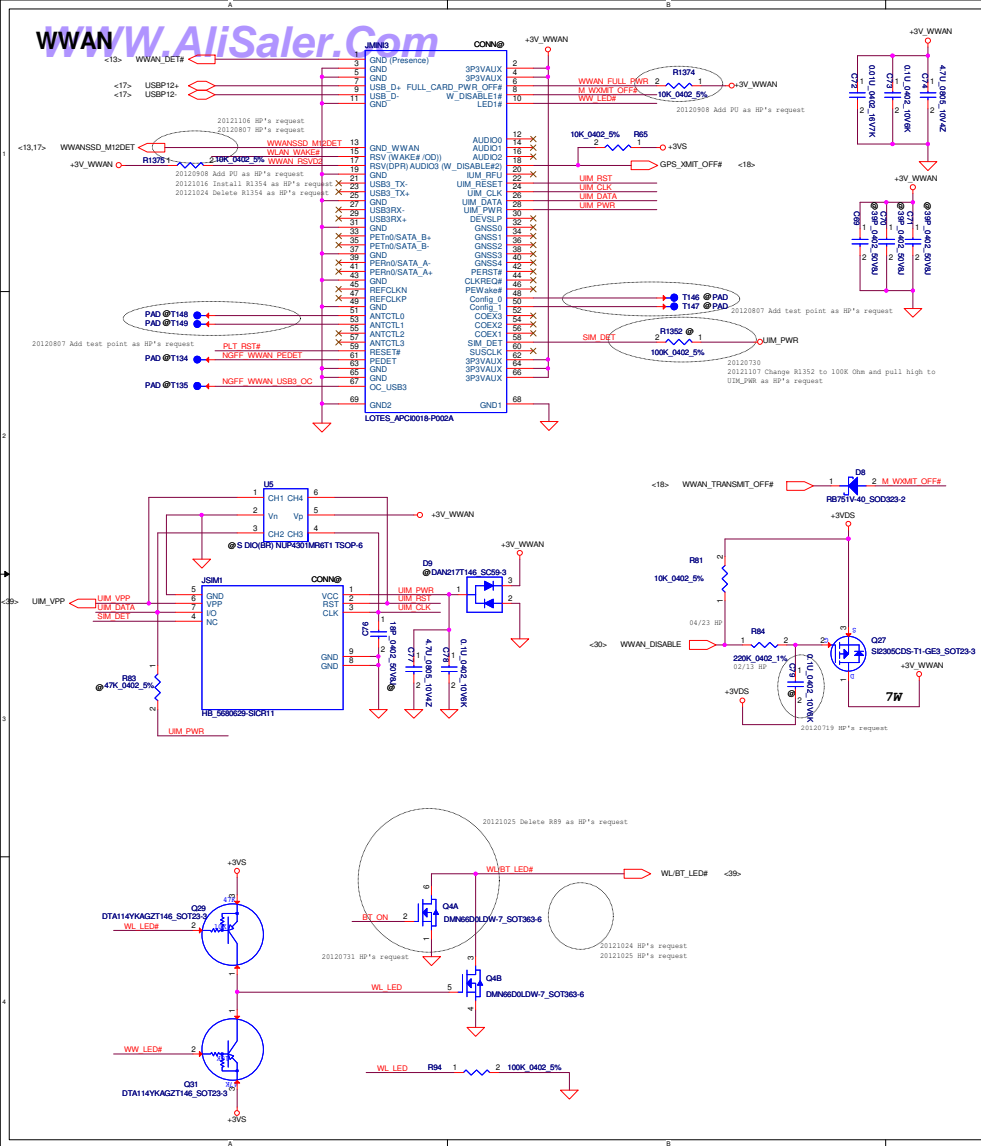
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	IBEX-M(IU/6)-HDA/JTAG/SATA
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				Date:	Monday, November 12, 2012
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## PWM Fan Control circuit

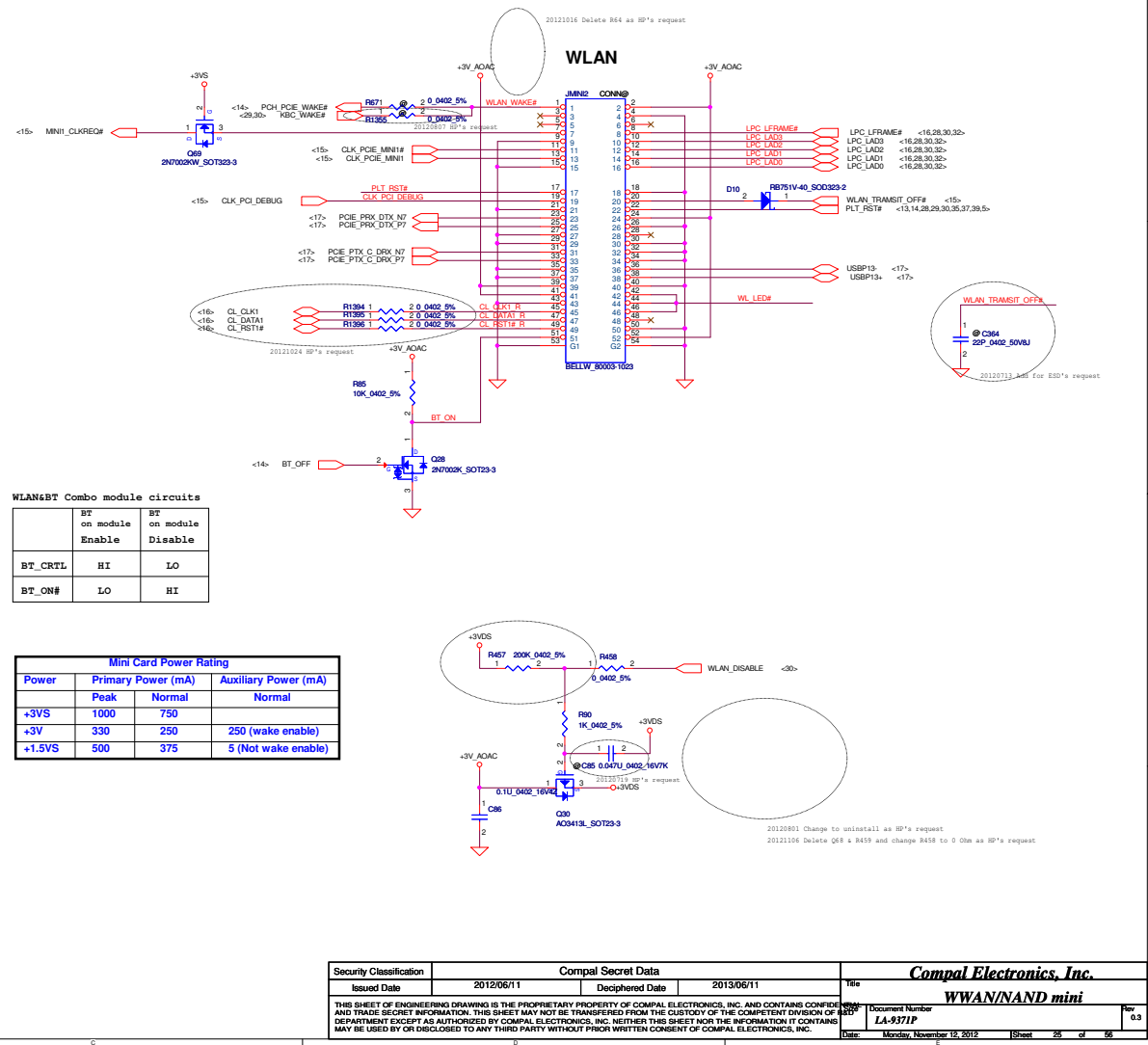


Security Classification	Compal Secret Data			Title	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Sandy(2/7) PM,XDP,Thermal	
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				LA-9371P	0.3
				Date: Monday, November 12, 2012	Sheet 24 of 56

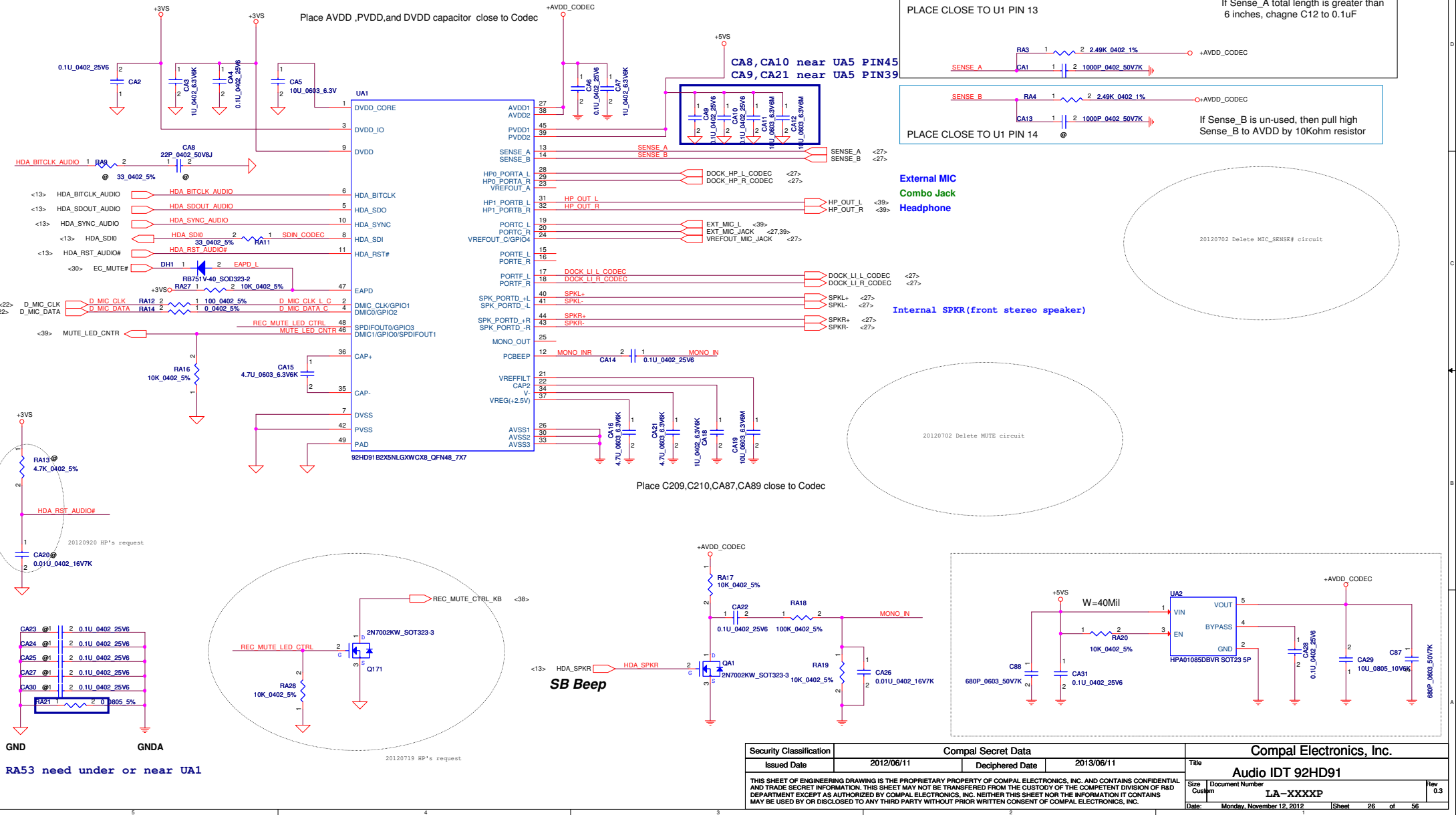




## WLAN

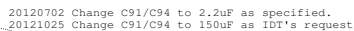
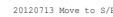


Notes:  
Keep PVDD supply and speaker traces routed on the DGND plane.  
Keep away from AGND and other analog signals





### *DOCK Audio*



20121011 IDT's suggestion

20121011 IDT's suggestion

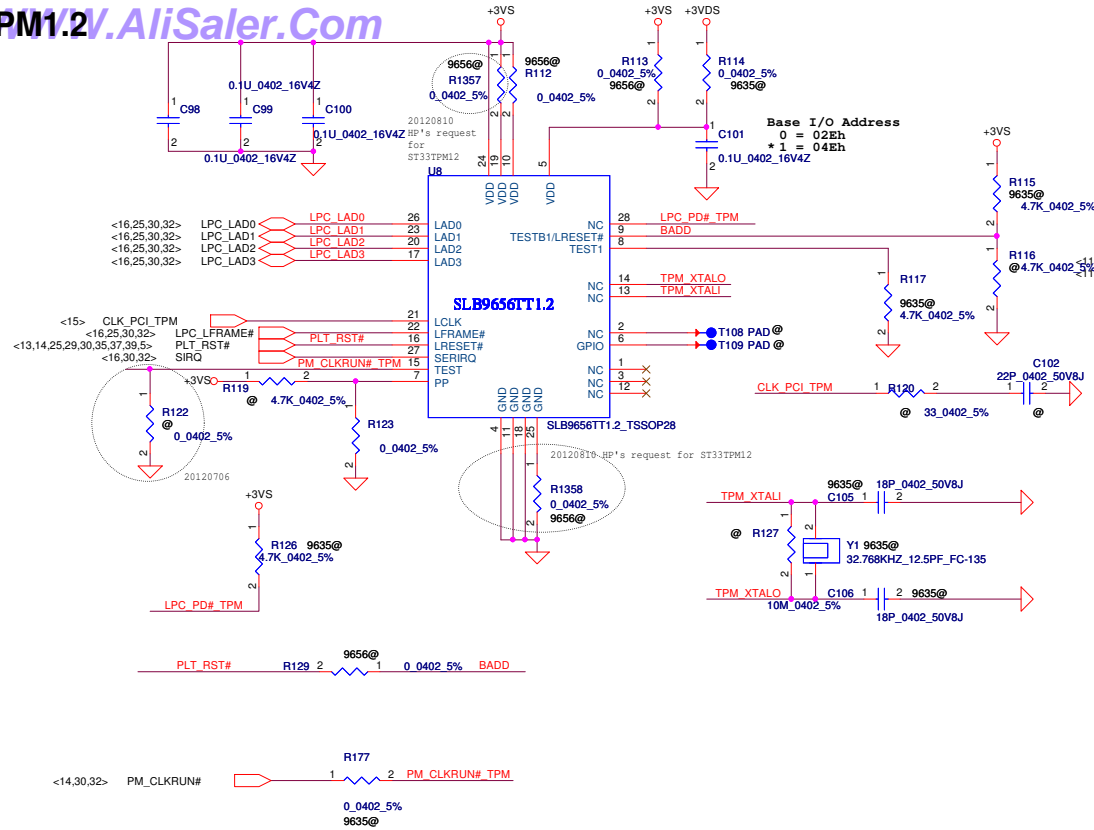
20121102 for N.O. type

20121011 IDT's suggestion

37% 1110

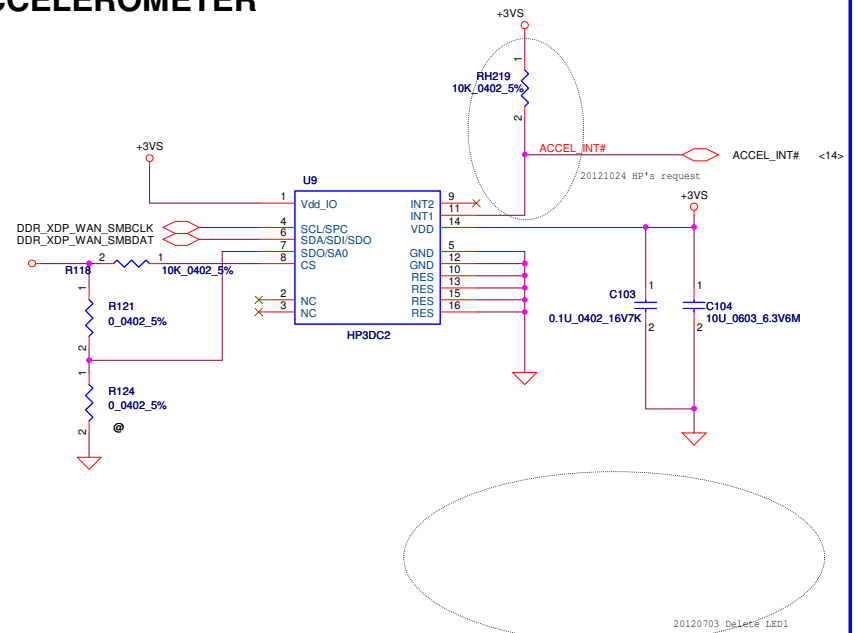
20121011 IDT's suggestion

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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Size	Document Number LA-9371P
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Date:		Monday, November 12, 2012		Sheet	27 of 56

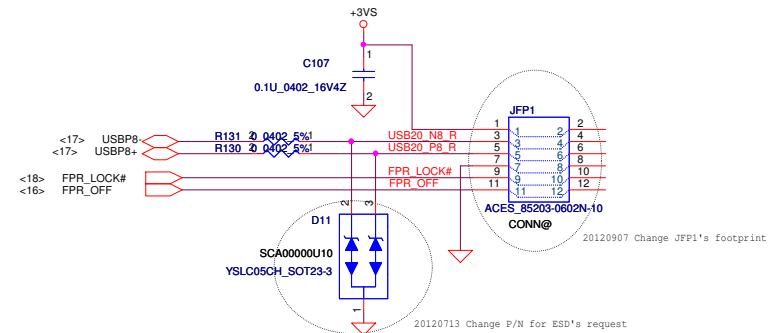


TPM	BOM Option (Not Install)
SLB9635	R112, R113, R129
SLB9656	R114, R115, R117, R126, R177, C105, C106, Y1
ST33TPM12	R113, R129, R114, R115, R117, R126, R177, R1357, R1358, R127, R122, R116, R120, C102, C101, C105, C106, Y1

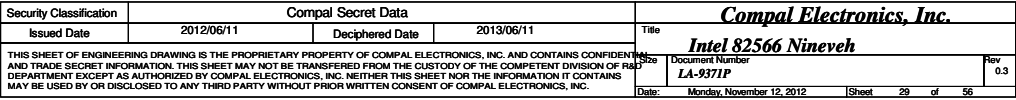
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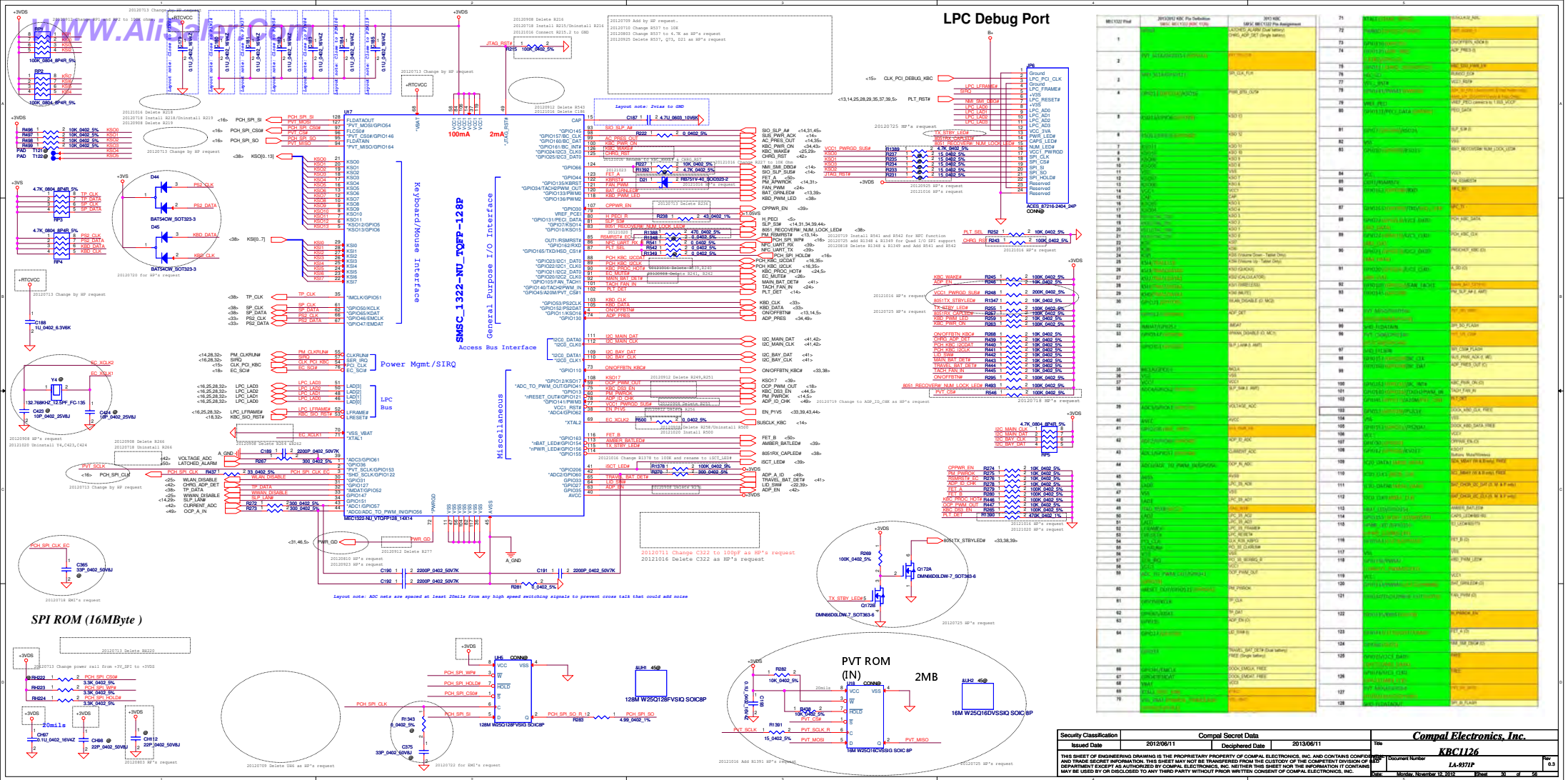


## Finger printer



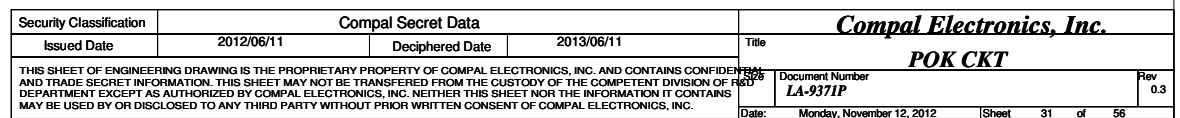
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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	<b>TPMI/Gsensor</b>	
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				Date:	Monday, November 12, 2012	Sheet 26 of 56



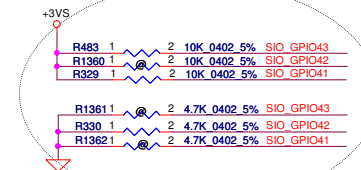
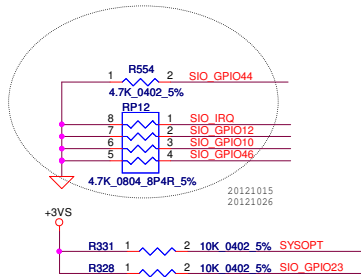
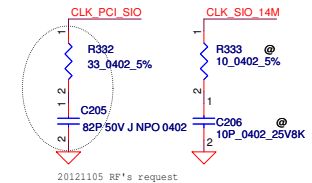
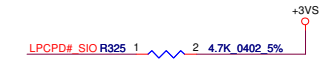
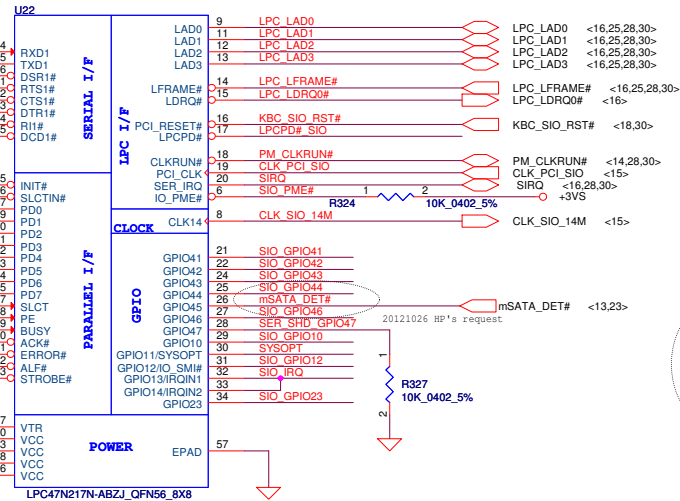
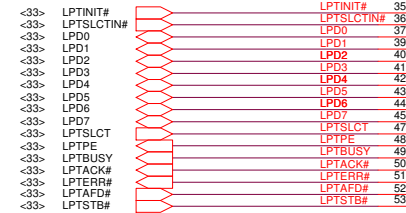
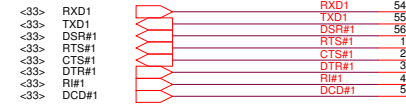
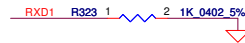
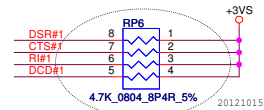
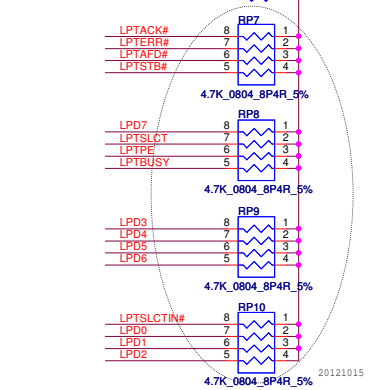


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				LA-831P		0.3
				Date	Monday, November 12, 2014	Sheet 30 of 30





+5VS\_PRN 



### Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3					
GPIO43	GPIO42	GPIO41	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
1	0	1	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	1	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8

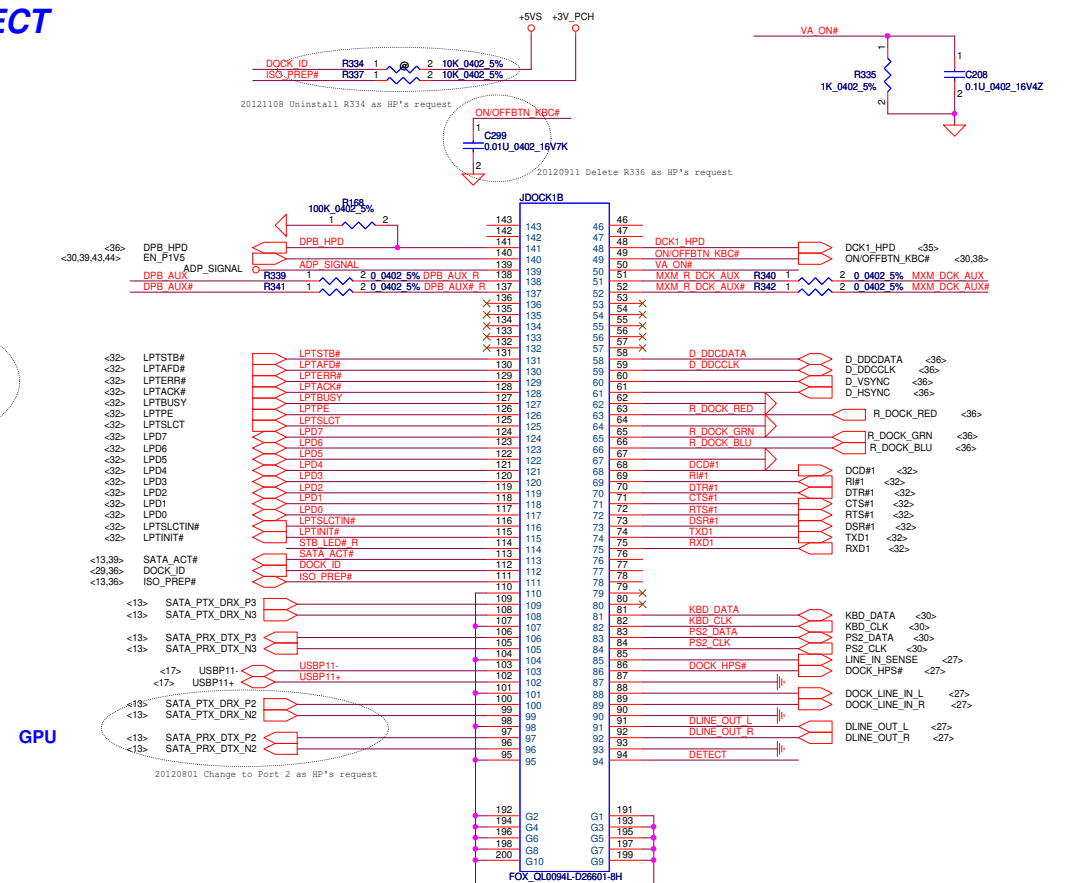
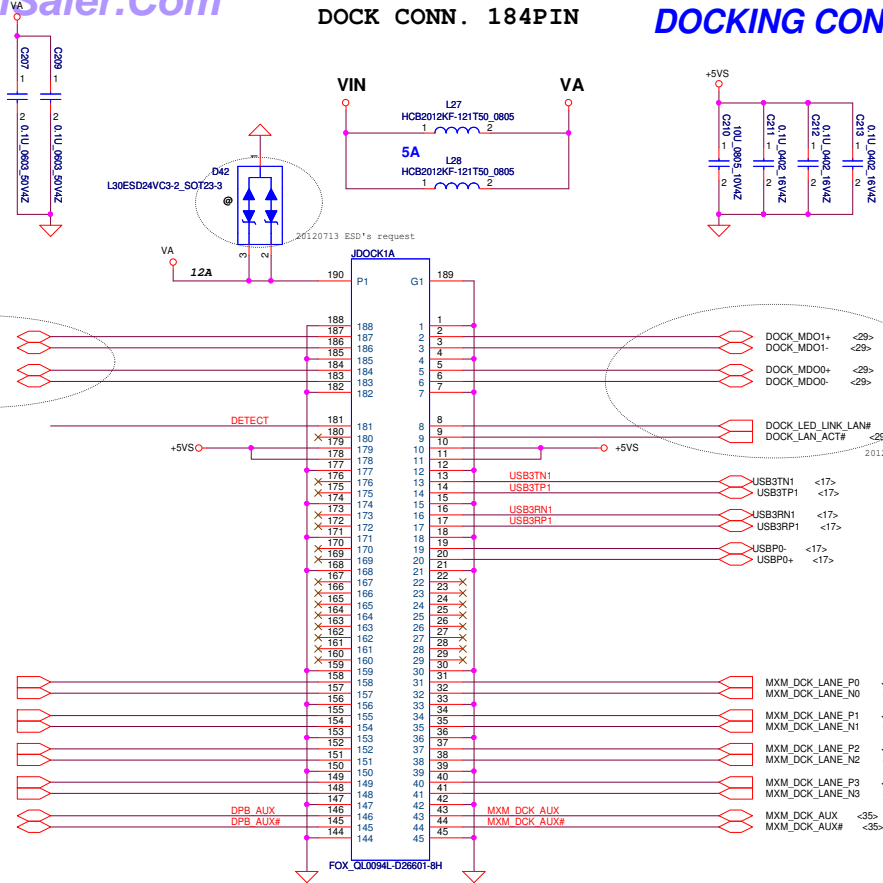
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>SUPER I/O LPC47N217N-ABZJ</b>	
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title	Rev 0.3
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# DOCK CONN. 184PIN

# DOCKING CONNECT

- (1) PCI Express x1 channels
- (2) P8/2 Interfaces
- (2) USB 2.channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface



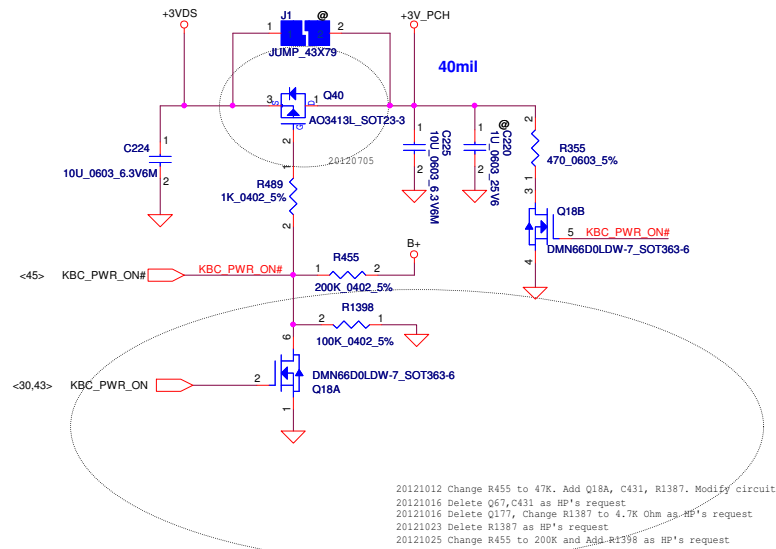
IN	NC<--->COM	NO<--->COM
L	ON	OFF
H	OFF	ON

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Issued Date	2012/06/11	Deciphered Date	2013/06/11
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Title		Compal Electronics, Inc.	
Size		Document Number	
Custom		LA-9371P	
Date		Monday, November 12, 2012	
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Rev		0.3	

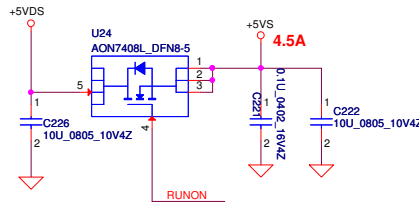
## WWW.AMPCORP.COM

### +3VALW to +3VALW(PCH AUX Power)

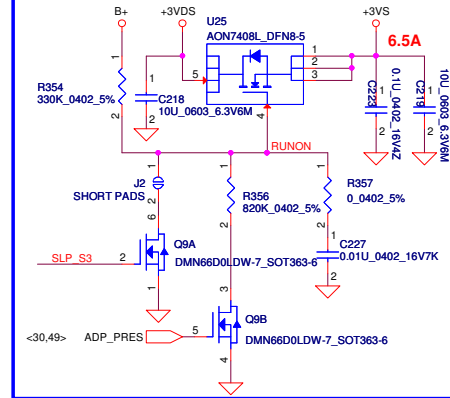
Short J1 for PCH VCCSUS3.3



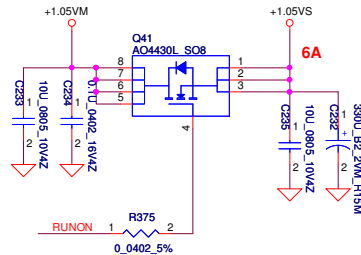
### +5VALW to +5VS Transfer



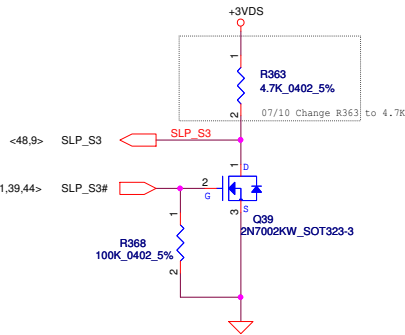
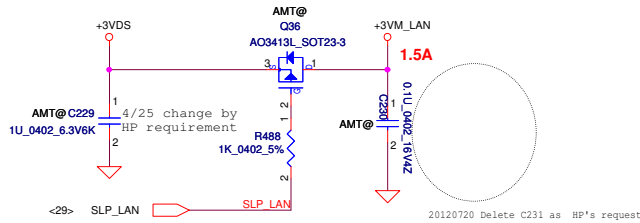
### +3VALW to +3VS Transfer



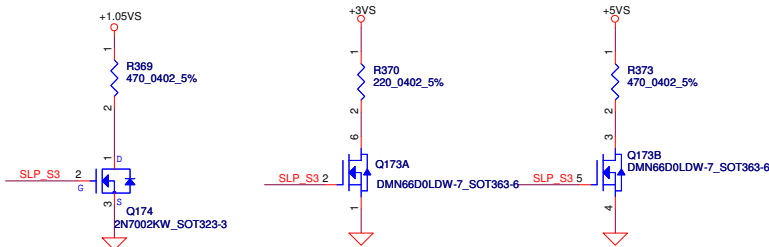
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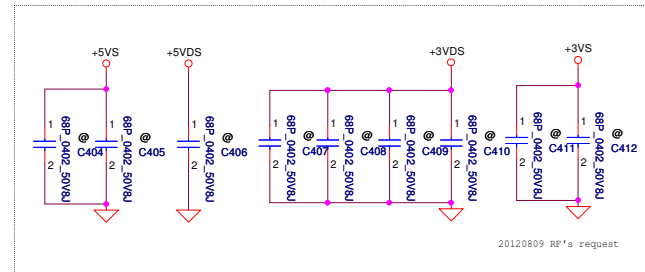
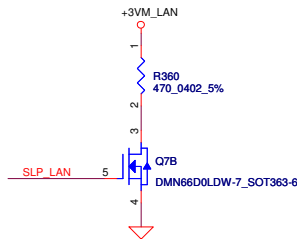
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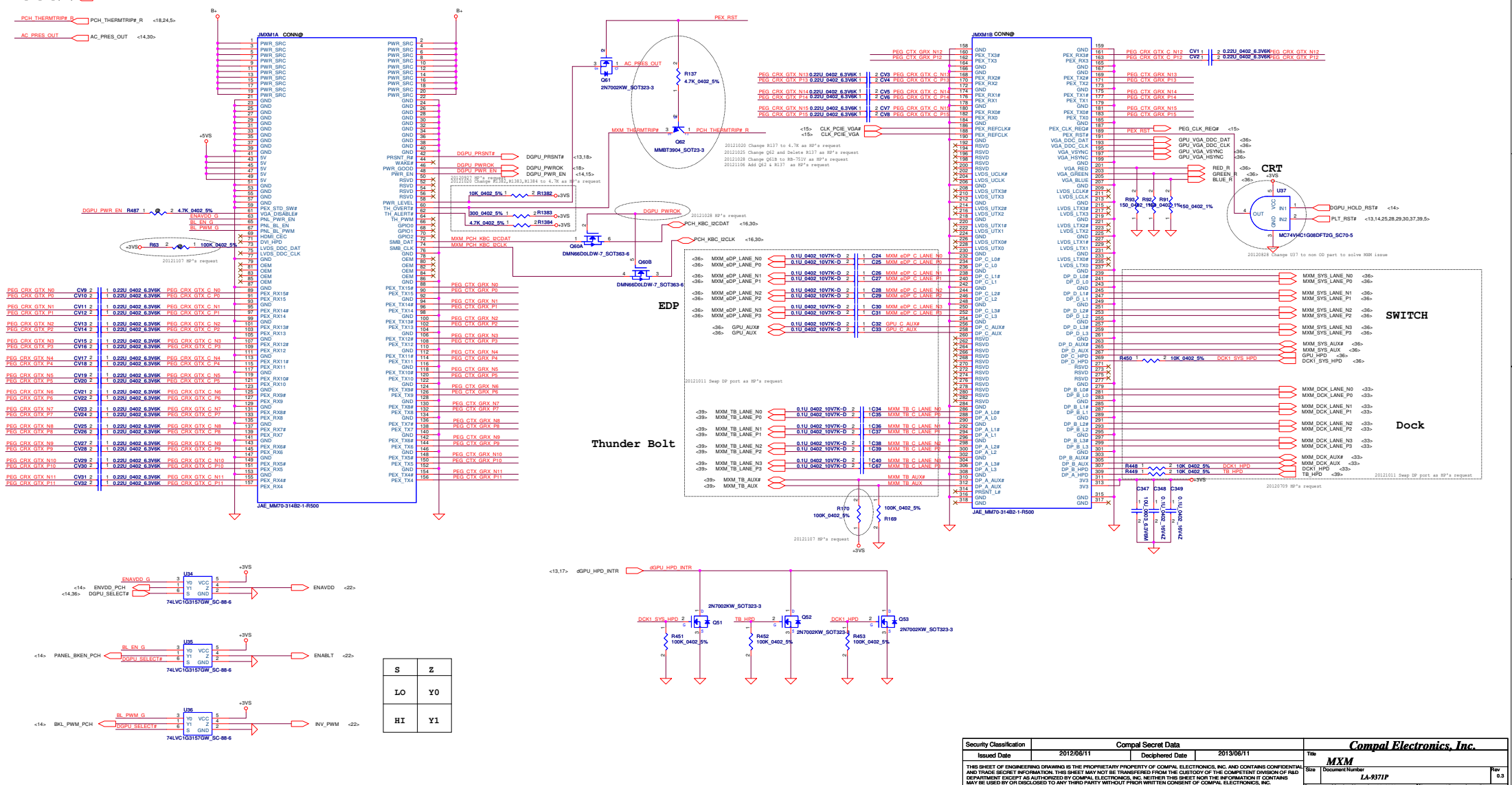


### Discharge circuit-1




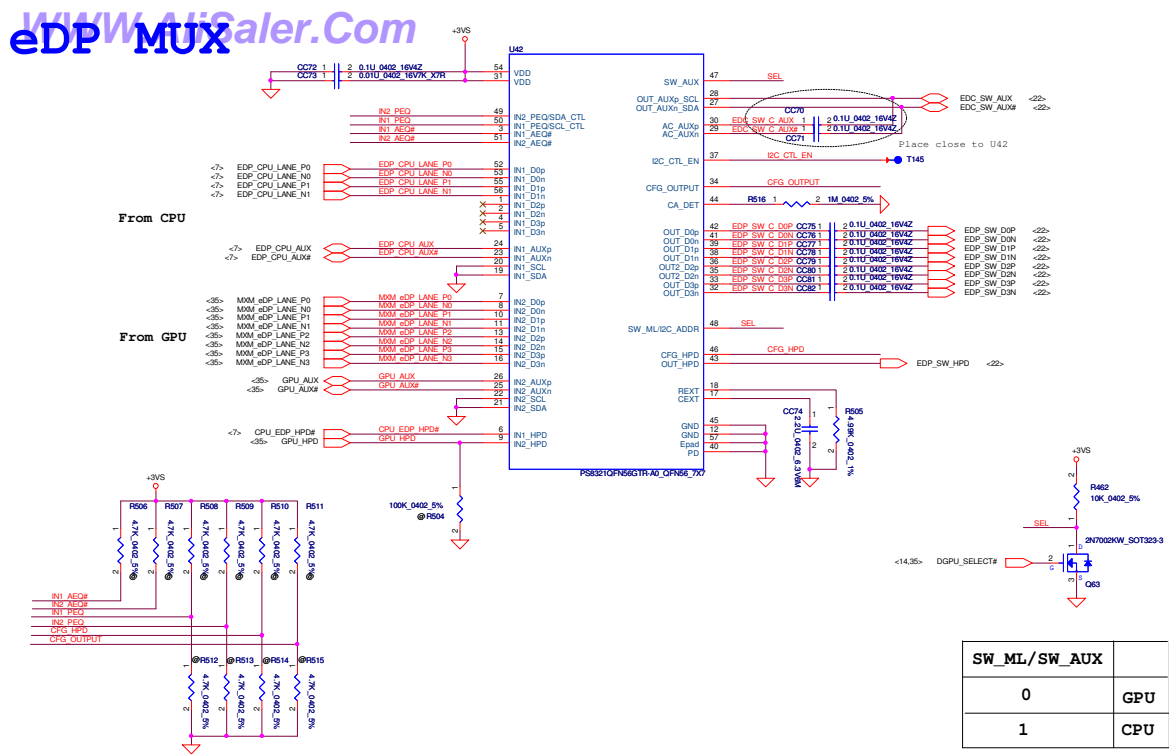
### Discharge circuit-2 for V-M



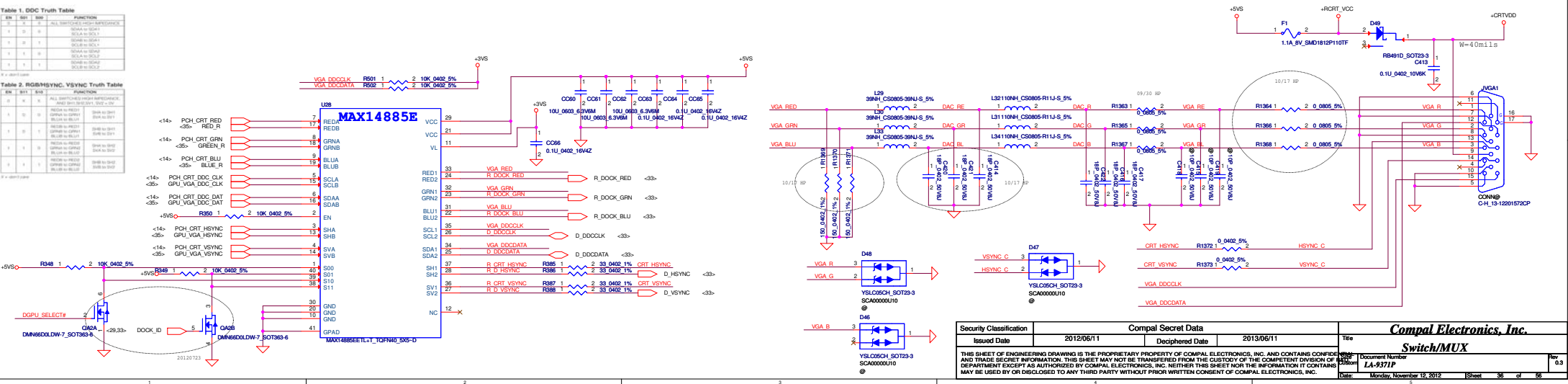
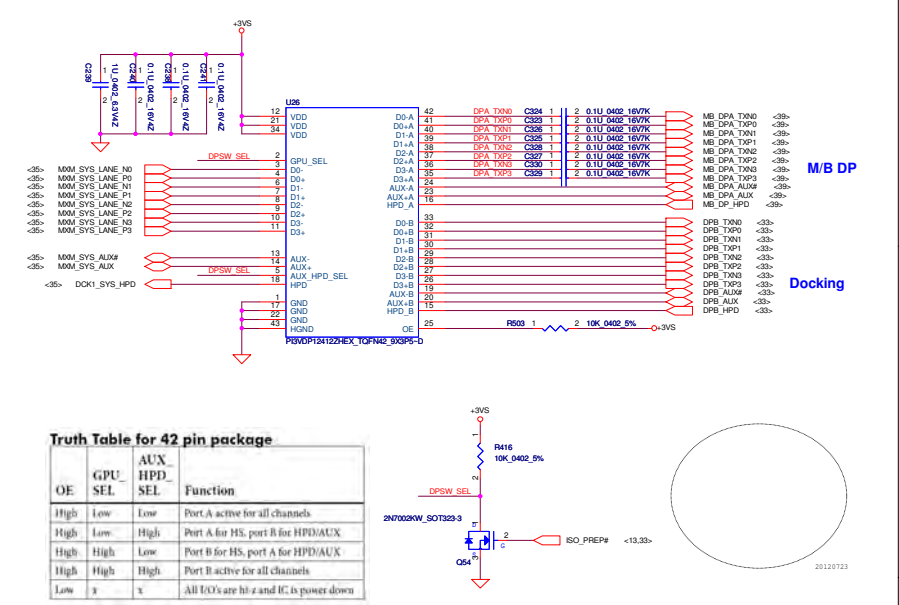


S	Z
LO	Y0
HI	Y1

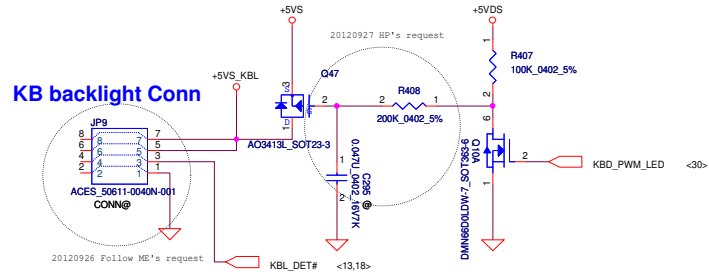
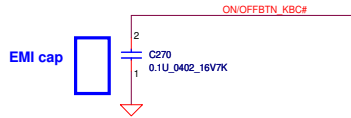
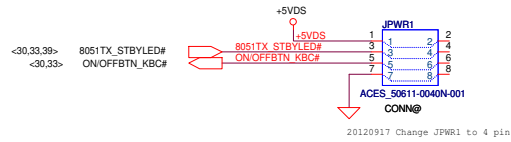
Security Classification		Compal Secret Data		<div><b>Compal Electronics, Inc.</b></div>		
Issued Date	2012/06/11	Decipher Date	2013/06/11	Title	<b>MXM</b>	
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				<b>LA-9317P</b>		0.3
				Date:	Monday, November 12, 2012	



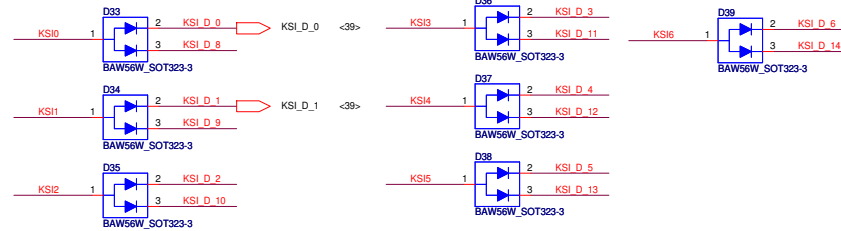
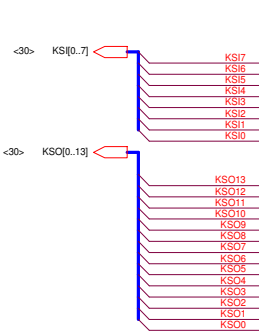
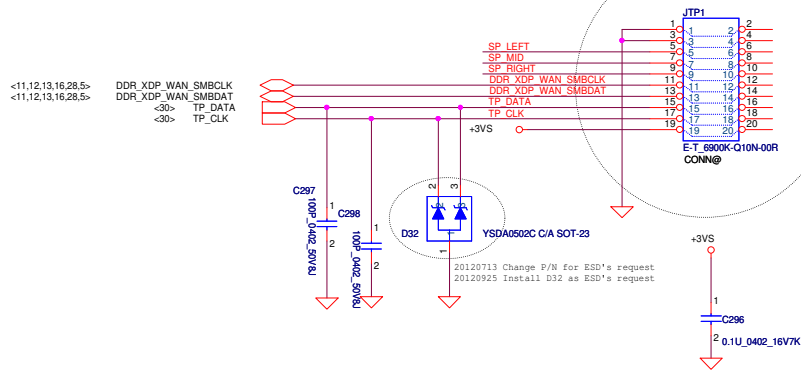
## DP Switch



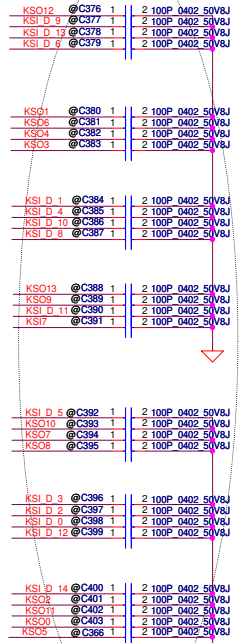
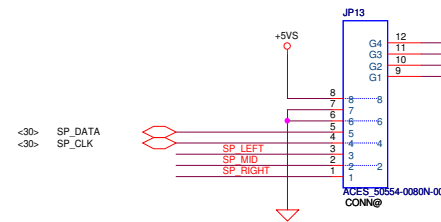




## TP/B TO M/B

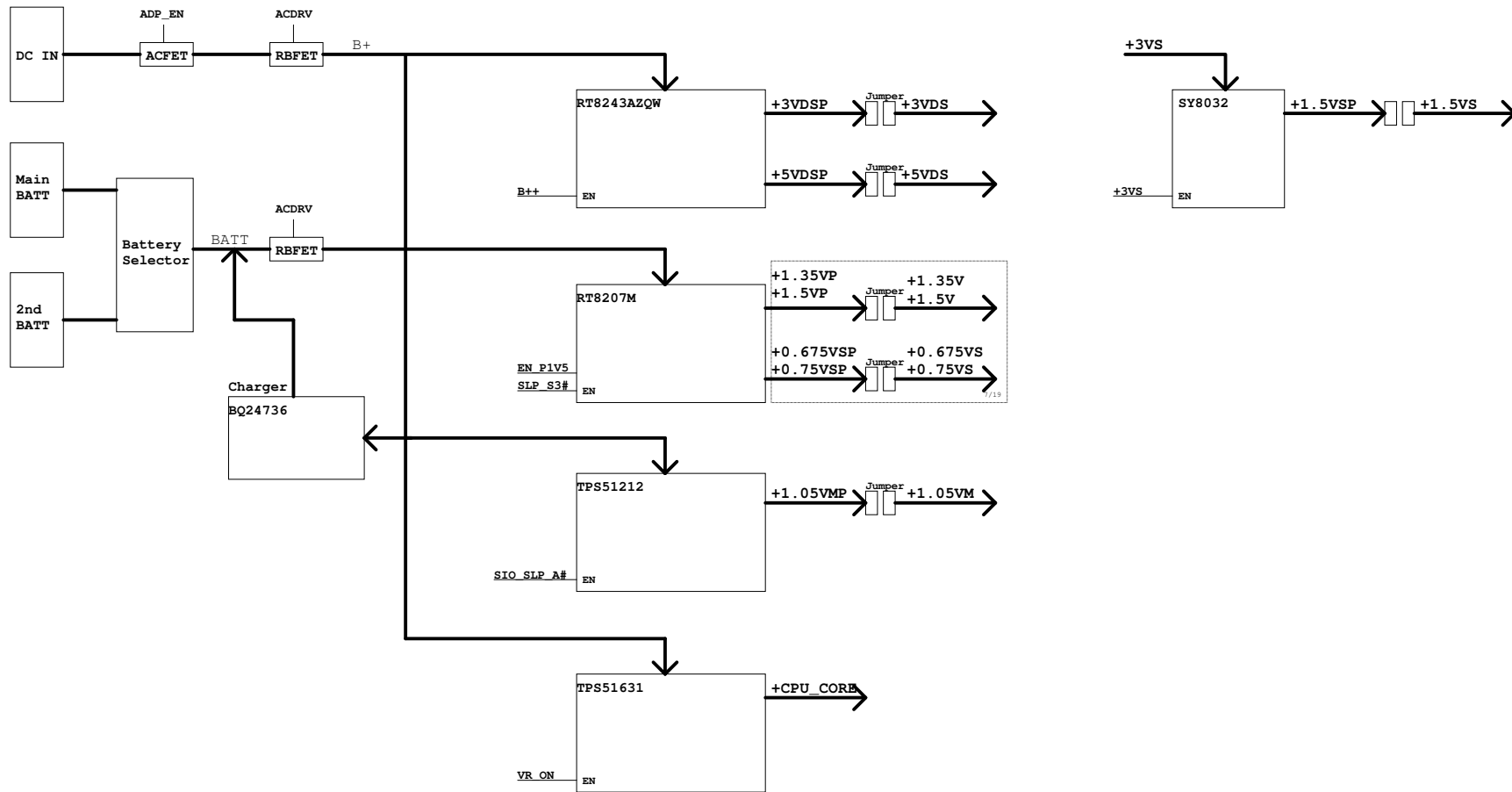


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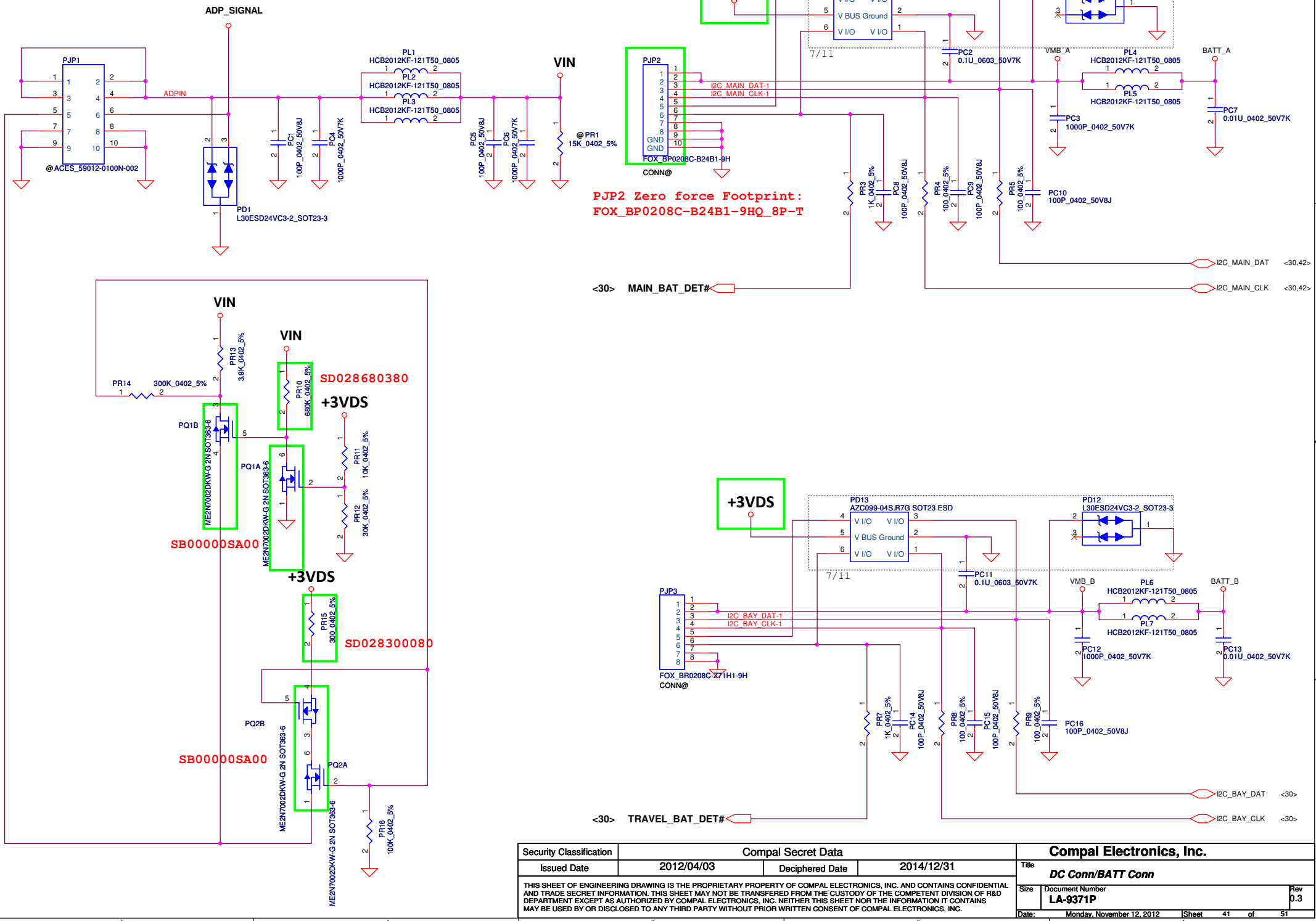


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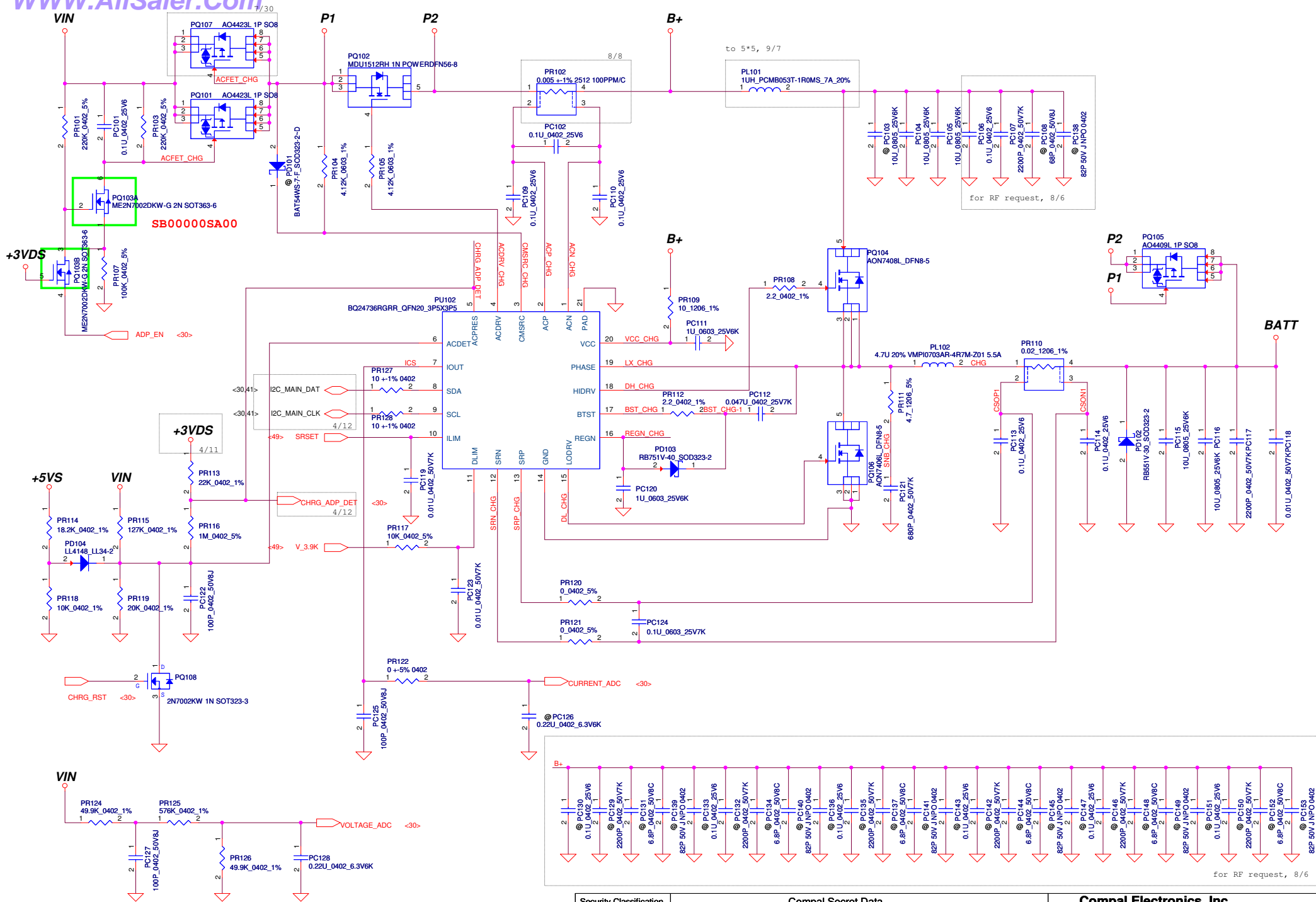






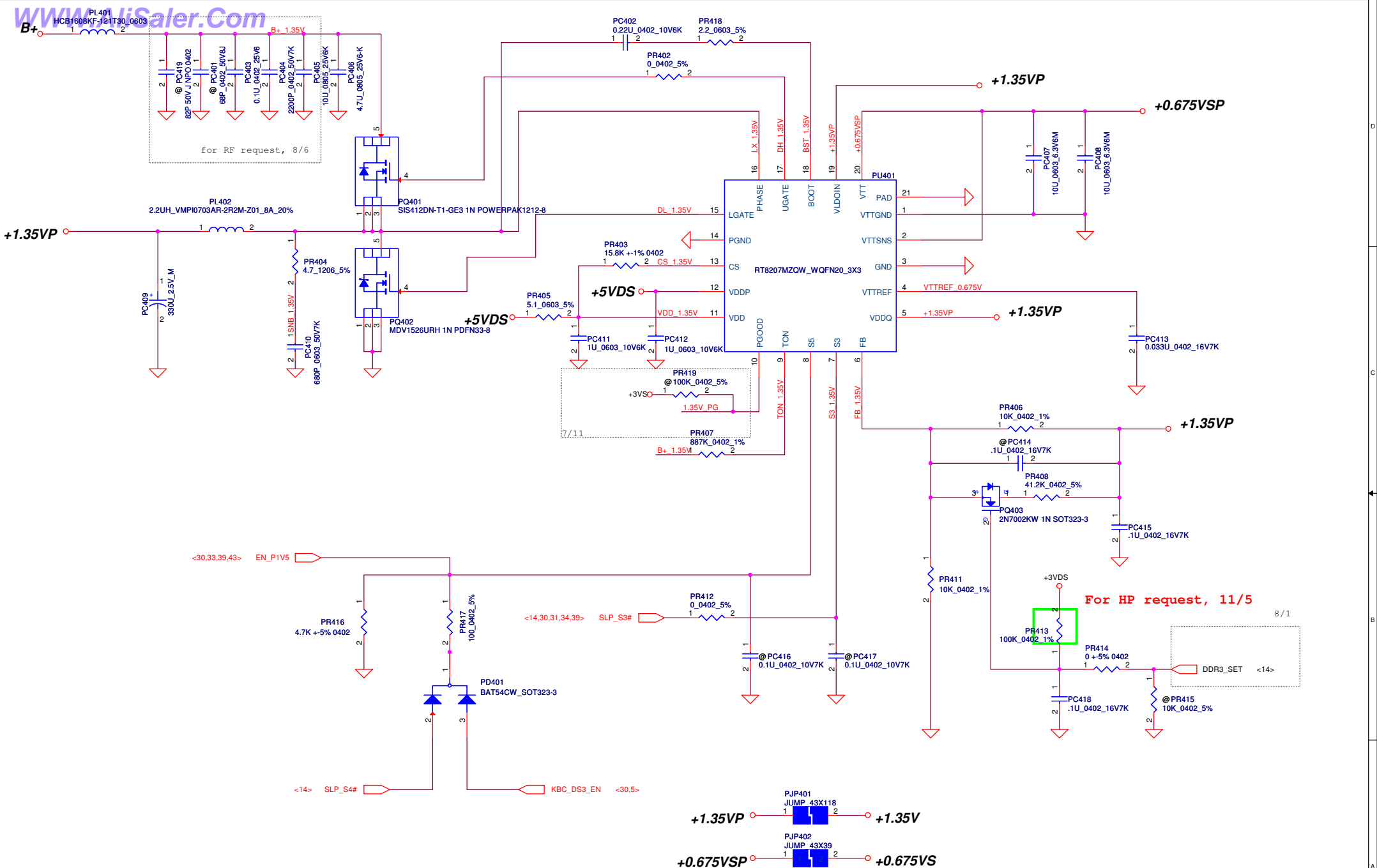


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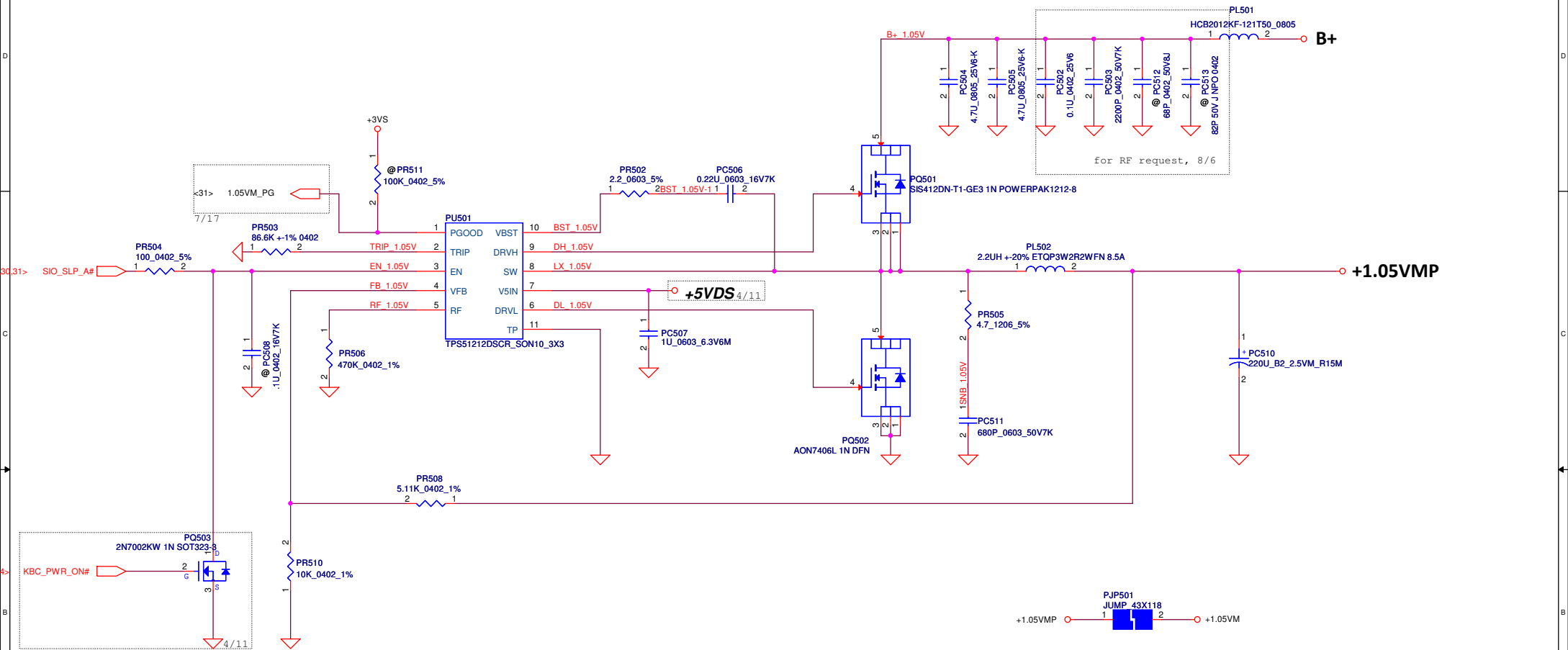


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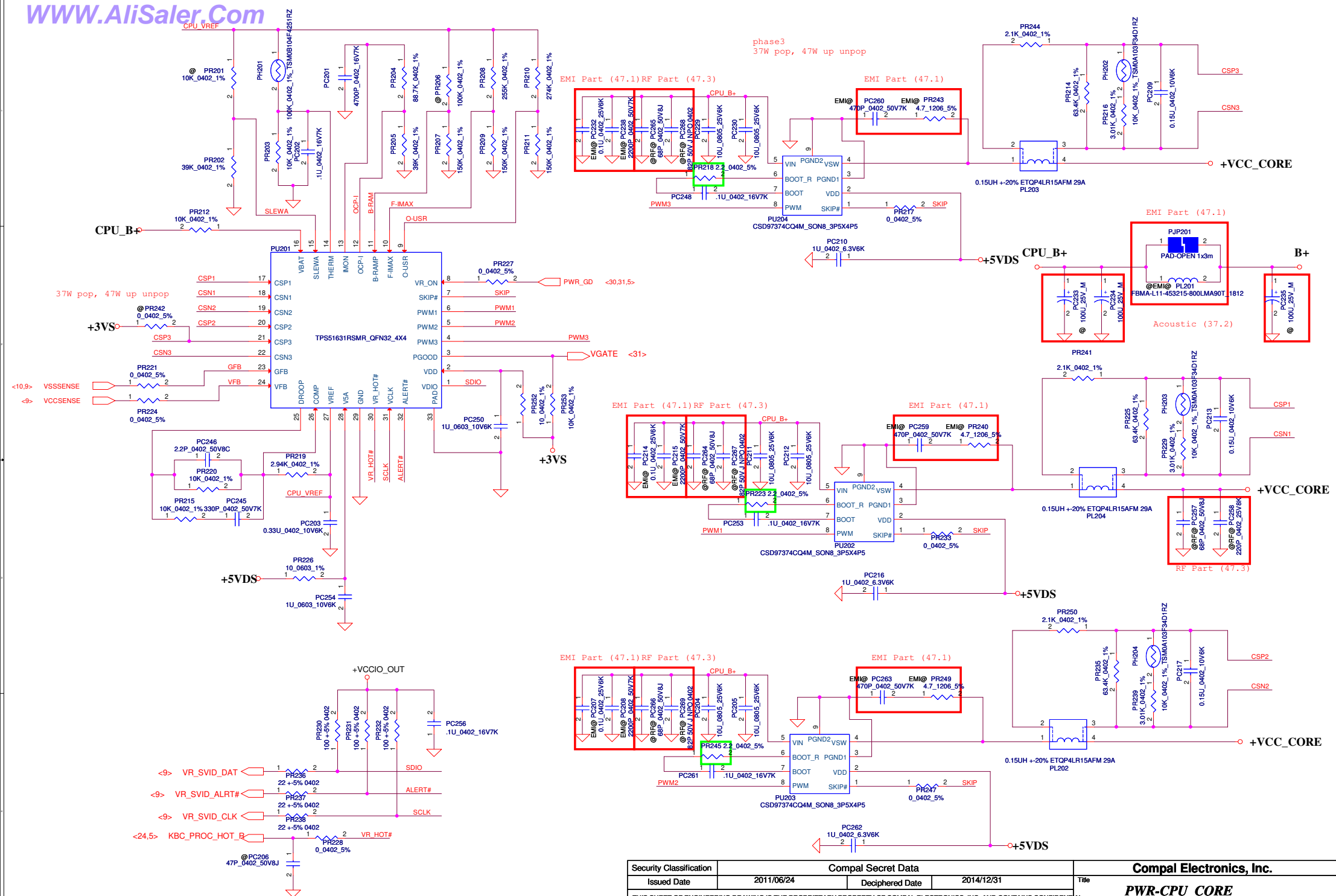




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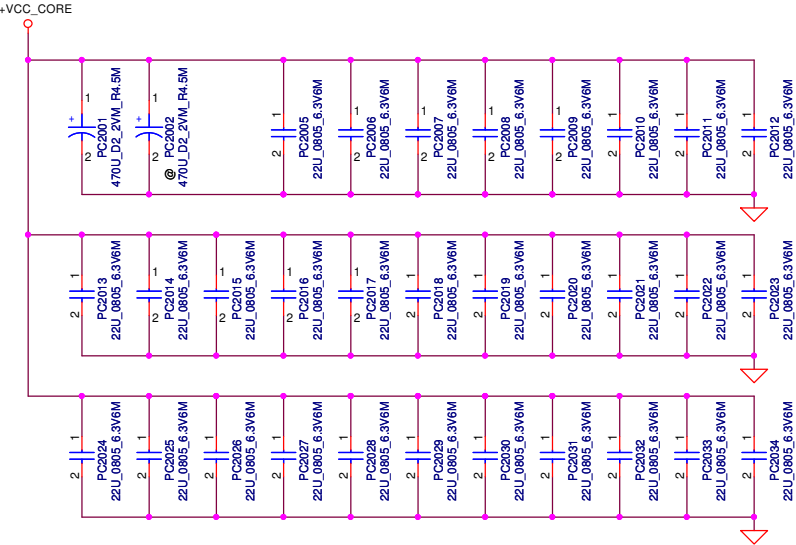


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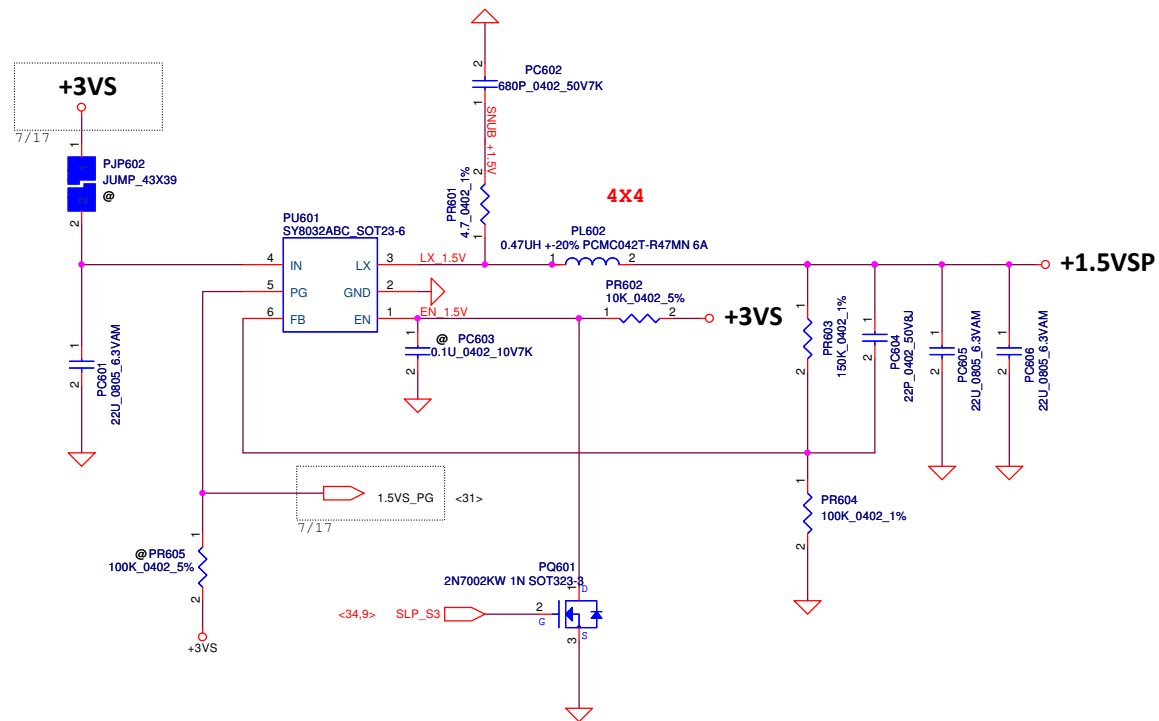


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+VCC\_CORE 2 X 470u/4m  
30 X 22u/0805



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+1.5VSP

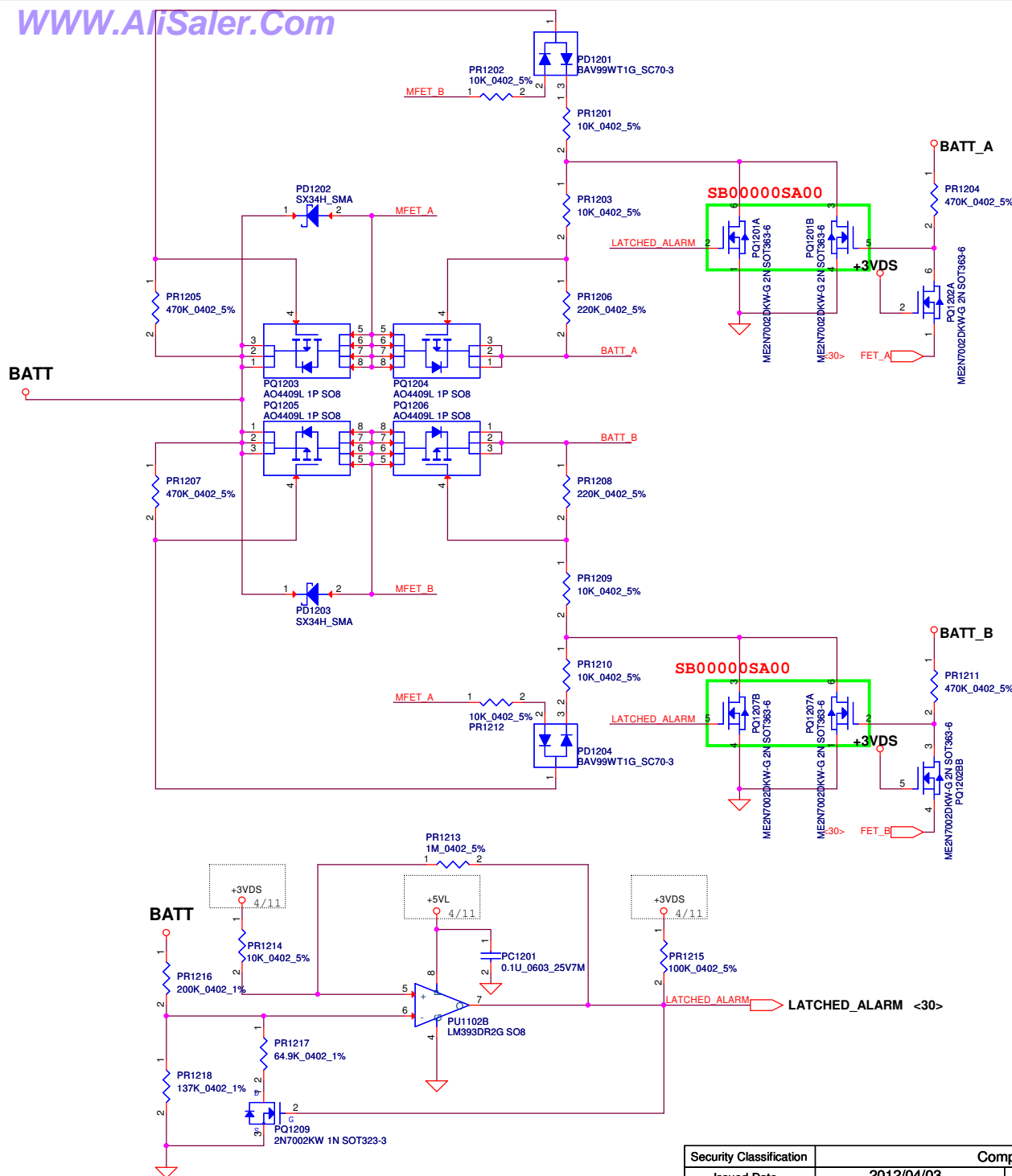
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+1.5V\_PCIEP  
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	Reserve PC130,129,131,139,133,132,134,140,136,135,137,141,143,142,144,145,146,147,148,149,151,150,152,153,138	2012/08/06		RF solution		
2	43	Reserve PC324,322,323,325326,327,328,329,330,331,302,303	2012/08/06		RF solution		
3	43	Add PC305,304,308,309	2012/08/06		RF solution		
4	44	Reserve PC419,401	2012/08/06		RF solution		
5	44	Add PC403,404,405	2012/08/06		RF solution		
6	45	Reserve PC512,513	2012/08/06		RF solution		
7	45	Add PC502,503	2012/08/06		RF solution		
8	47	Reserve PC264,267,266,269,265,268	2012/08/06		RF solution		
9	47	Add PC214,215,207,203,232,236	2012/08/06		RF solution		
10	47	Change PC233,234 from SF000001280 to SF000004M00	2012/08/09		Change the hieght to 6mm		
11	46	Change PR234 from 19.1K to 62K	2012/08/10		HP suggestion		
12	47	Change PQ203,204,211 from SB00000K300 to SB00000U200	2002/09/11		Design change		
13	47	Change PQ201,205,209 from SB00000SJ00 to SB00000W200	2002/09/13		Design change		
14	43	Change PQ301,302 from SB00000JM00 to SB00000IA00	2012/09/17		Design change		
15	43	Change PQ303 from SB00000CT00 to SB00000H700	2012/09/17		Design change		
16	43	Change PQ304 from SB00000N800 to SB00000TZ00	2012/09/17		Design change		
17	44	Change PQ401 from SB00000H800 to SB00000IA00	2012/09/17		Design change		
18	44	Change PQ402 from SB00000N800 to SB00000TZ00	2012/09/17		Design change		
19	45	Change PQ501 from SB00000H800 to SB00000IA00	2012/09/17		Design change		
20	45	Change PQ502 from SB00000N800 to SB00000H700	2012/09/17		Design change		
21	50	Reserve PR1101,1102,1103,1104,1105,1106,1107,PC1100,1102,PD1101	2012/10/2		HP suggestion		
22	44	Change PD401 from SC600000D00 to SCS00006400	2012/10/2		HP suggestion		
23	44	Change PR416 from SD034100380 to SD028470180	2012/10/2		HP suggestion		
24	42	Change PL101 from SH00000MR00 to SH00000NW00	2012/10/2		Design change		
25	47	Change PR240,243,249 from SD001470B80 to SD000010280	2002/10/2		Design change		
26	47	Change PC233 from SF000001280 to SF000004M00	2012/10/2		Design change		

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## Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & R1349 and Add R541 and R542	0.2
2	31	PWR_OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262, R266, R219, R216, R241, R242, R271, R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_VART_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU_AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU_AL34 pin to H_CPU_PWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 directly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107, RH103, RH114, RH116, RH122 RH124, RH126, RH127, RH129, RH130	0.2
18	14	PCH	09/11	HP	Reassignment GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249, R251, R256, R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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## Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	29	LAN	09/12	HP	Avoid IEEE failure with trace stub lines	Add Lan switch solution PI3L500-AZFEX (U43)	0.2
24	39	I/O CONN	09/12	HP	Move Hall sensor IC on Function board	Add +3VDS & LID_SW# pin to JFB1	0.2
25	22	eDP	09/13	Compal	Avoid LVDS Burn out Risk	Rearrange pin assignment of JEDP1	0.2
26	31	POK CKT	09/13	HP	Modify Power OK circuit	Delete VH7, RJ235 ; Add RJ379	0.2
27	39	I/O CONN	09/19	HP	Prevent Card Reader can't be recognized issue	Add RJ380 for PCH_PCIE_WAKE#	0.2
28	13	PCH	09/19	HP	Disable the unlock of ME descriptor	Change QH11 to P-MOSFET	0.2
29	37	Smart Card	09/20	HP	RC delay is NOT good as reset	Delete CC67, RJ393, then connect U30.23 to PLT_RST#.	0.2
30	26	CODEC	09/20	HP		Uninstall RA13 and CA20	0.2
31	14	PCH	09/20	HP	KBC appears drives high during S3, so the change to avoid the leakage without losing functionality.	Change RH74 from 10K to 100K Ohm	0.2
32	31	PWR OK	09/23	HP	Modify net name for easy read	Modify VR_ON to PWR_GD and PWR_GOOD_3 to VGATE	0.2
33	5	XDP	09/25	HP		Connect PM_PWROK to JXDP1.47 via 0 Ohm (RC107)	0.2
34	30	KBC	09/25	HP	Resolve ME LAN failures	Delete R537, Q73, D21	0.2
35	35	MXM	09/27	HP	There is yellow bang in device manager	Add pull high resistor (RJ382, RJ383 & RJ384) to +3VS	0.2
36	38	KB Backlight	09/27	HP		Change R408 to 200K Ohm, and uninstall C295	0.2
37	35	MXM	10/11	HP	Certain ports have better drive strength than others when the system is in DC mode	DP port re-assignment	0.3
38	26,27	CODEC	10/11	IDT		Change RA14 to 0Ohm, C95 to 0.47uF, R97, R98, RJ102, RJ104 to 1%	0.3
39	5,14 30,34	KBC	10/12	HP	To enable Intel Deep SX	Reserve RC108, VH6, CH113, RJ388. Change U17.85 and RJ388 connection netname to RSMRST#_EC. Change R455 to 47K, Add Q18A, C431, RJ387. Modify +3V_PCH power circuit	0.3
40	9	CPU	10/16	HP	To enable Intel Deep SX	Add QC6 and connect to KBC_PWRON	0.3
41	41	CPU	10/16	HP	To enable Intel Deep SX	Add Q176 and add connection to PLT_DET	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																													
42	25	WLAN	10/16	HP	To enable Intel Deep SX	Delete R64, Install R1354	0.3																													
43	29	LAN	10/16	HP	To enable Intel Deep SX	Change connection of R1359 to KBC_WAKE#	0.3																													
44	30	KBC	10/16	HP	To enable Intel Deep SX	Change R227 to 3.3K	0.3																													
45	30	KBC	10/16	HP	To enable Intel Deep SX	Connect R215.2 to GND, Delete C186	0.3																													
46	30	KBC	10/16	HP	To enable Intel Deep SX	Remove current VCC1_PWRGD connection to JP6.16. Then add a 4.7 K resistor between JP6.16 and new signal VCC1_PWRGD_SUS#.	0.3																													
47	30	KBC	10/16	HP	To enable Intel Deep SX	Rename CHARGER_CLK & CHARGER_DAT to KBC_WAKE# & CHRGR_RST	0.3																													
48	30,39	KBC & I/O	10/16	HP	To enable Intel Deep SX	Change R1378 to 100K and rename U17.41 to iSCT_LED# Delete C322 Change JTB1.98 to iSCT_LED#.	0.3																													
49	30	KBC	10/16	HP		add R1391between U18.6 pin and signal PVT_SCLK	0.3																													
50	30	KBC	10/16	HP	Simplify the KBC circuit	Connect R215.2 to GND, Delete C186 Change R227 to 10K Delete R239, R240 and connect to KBC (U17) directly. Delete R218 and connect to KBC (U17) directly.	0.3																													
51	30	KBC	10/16	HP	Simplify the KBC circuit	Delete R1381 and connect JCR1.5 to +5VDS.	0.3																													
52	5,9,14 16,20,24 25,30, 34,35	KBC	10/20	HP		Change R615 to 470K, R610 to 470Ohm and RH247 to 10K Change R1387,R137,R1382,R1383,R1384 to 4.7K, RC108 to 10K, Delete Q177,QC1,RC12,QC5B,QC6B,R461,Q2,RC90. Install RH209, R492, RC108, RH246, CH113 and VH6. Uninstall QC3, RH148, RH67, RH208. Change R492.2 connection to PCH_THERMTRIP#_R Connect RH247.1 to PM_RSMRST#. Modify +1.35VS power circuit	0.3																													
53	14	PCH	10/20	Compal	To solve bring up issue	Add PU resistor (RH248) for GPIO72	0.3																													
54	14,30,34	PCH	10/23	Compal	HP Deep SX implementation	Delete R1387, Uninstall RH246,CH113,VH6,RH209,Q176,RH247 Install RH67,RH208 ;Add 4.7K (R1392) between KBC 124 pin and signal SIO_SLP_SUS#.	0.3																													
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## Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
55	14,39	PCH, I/O	10/23	HP	For Intel ThunderBolt REDWOOD	Change PCH.AL6 to TBT_RR_GPIO# Change RH245.2 to TBT_RR_GPIO# Change JTB1.98 to TBT_RR_GPIO#	0.3
56	39	I/O	10/23	HP	For iSCT_LED# function	Add Q177 for control HDD & Wireless LED	0.3
57	25	Wireless LED	10/24	HP	Create about 1.36V with 47K PU when WL LED is off	Add PD 33K (R1393) for WL/BT_LED#	0.3
58	28	G-Sensor	10/24	HP	Current connection is incorrect	Connect ACCEL_INT# to U9 's pin11 and leave pin 9 as NC	0.3
59	18	PCH	10/24	HP		Connect RH176.2 to GND (from +3VS) and install RH176 Install RH185	0.3
60	25	WLAN	10/24	HP		Add serial resistor R1394, R1395, R1396 for CLINK signals	0.3
61	14	PCH	10/25	HP		Add RH249 for SLP_LAN# and change RH70 to 200K	0.3
62	14,29	PCH, LAN	10/25	HP	To provide isolation	Add PU RH250 for LANWAKE# and Q177 for isolation	0.3
63	25	WLAN	10/25	HP		Delete R89 and R1393	0.3
64	39	I/O	10/25	HP	For iSCT_LED# function	Change Q178 to BSS138 and Add R1393	0.3
65	35	MXM	10/25	HP	For MXM GPIO8 issue	Combine Q61/Q62 to Dual 2N7002 (Q61) and Delete R137	0.3
66	34	DC-DC	10/25	HP	S5 power consumption concern.	Change R455 to 200K and add PD 100K (R1398)	0.3
67	29	LAN	10/26	HP	+5VDS may disappear during Deep S4/S5	Connect R376.1 to +3VDS and change R376 to 10K	0.3
68	29	LAN	10/26	HP		Connect DOCK_LED_LINK_LAN# to Q34.1 and delete R153	0.3
69	18,32	PCH, Super I/O	10/26	HP		Reassign Super I/O GPIO45 as mSATA_DET#	0.3
70	17	PCH	10/26	HP		Reassign GPIO59 as WWAN_DET#_PCH and connect to JMINI3	0.3
71	13	PCH	10/26	HP		Swap QH11A.2 and QH11B.5 connection	0.3
72	35	MXM	10/28	HP	For MXM GPIO8/GPIO9 issue	Change MOS to Diode RB-751(D5) and R1383 to 300 Ohm	0.3
73	35	MXM	10/28	HP		Connect Q60 pin 2 & pin 5 to DGPU_PWROK	0.3
74	31	PWROK	10/31	HP	To ensure +5VDS power off	Connect R291.1 to +5VL and change it to 105K Ohm	0.3
75	39	I/O	10/31	HP		Change JCR1.48 & 50 from +3VDS to +3VS	0.3
76	29	LAN	11/2	HP	Avoid NIC internal PHY voltage drop	Reserve 10uF (C428) & change C351 to 47uF	0.3
77	27	Audio	11/2	Compal	OBS#894504- SVTP-DB1R_AB1.0: Can't record sound via audio jack with external headphone	Delete Q1AB & R174 then connect HP_SENSE# to R167	0.3
78	9	CPU	11/4	Compal		Change connection of QC5A.2 & QC5B.5 to SLP_S3	0.3

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